

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-DIS/11/6883 Notification Date 11/14/2011

APM - ASD & IPAD Division

Schottky Diodes and DIACs in DO-35/MELF/MiniMELF packages Relocation of the assembly and test within China

Table 1.	Change	Implementation	Schedule
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Forecasted implementation date for change	23-Jan-2012
Forecasted availabillity date of samples for customer	01-Jan-2012
Forecasted date for STMicroelectronics change Qualification Plan results availability	23-Jan-2012
Estimated date of changed product first shipment	13-Feb-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	Schottky Diodes and DIACs in DO-35/MELF/MiniMELF
Type of change	Package assembly location change
Reason for change	to expand our manufacturing capacity
Description of the change	This document is to inform of the assembly and test relocation of our Signal Schottky Diodes and DIACs in DO-35, MELF and MiniMELF packages within China. This transfer to a new plant located 150 km away from the current site will offer the possibility of expanding our manufacturing capacity on the considered products.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	internal codification and QA number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

	>\$
Customer Acknowledgement of Receipt	PCN APM-DIS/11/6883
Please sign and return to STMicroelectronics Sales Office	Notification Date 11/14/2011
Qualification Plan Denied	Name:
Qualification Plan Approved	Title:
	Company:
🗖 Change Denied	Date:
Change Approved	Signature:
Remark	

Name	Function	
Paris, Eric	Division Marketing Manager	
Duclos, Franck	Division Product Manager	
Cazaubon, Guy	Division Q.A. Manager	

DOCUMENT APPROVAL



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-DIS/11/6883

APM - ASD & IPAD¹ Division

Schottky Diodes and DIACs in DO-35/MELF/MiniMELF packages:

Relocation of the assembly and test within China



(1) APM: Analog, Power & MEMS Group - ASD: Application Specific Device - IPAD: Integrated Passive and Active Devices

WHY THIS CHANGE?

This document is to inform of the **assembly and test** relocation of our **Signal Schottky Diodes** and **DIACs** in **DO-35**, **MELF** and **MiniMELF** packages within China.

This relocation to a **new plant** located 150 km away from the current site will offer the possibility of expanding our **manufacturing capacity** on the considered products.

The products involved are all the **Signal Schottky Diodes** and **DIAC families listed below**:

Product Family	DO-35 families	Mini MELF	MELF
Signal Schottlar	1Nxxx	TMMBAR28FILM	-
Diodes	BARxxx	-	TMBYV10-xxx
	BATxxx	TMMBATxxx	TMBATxxx
	DB3xxx	TMMDB3xxx	-
DIACS	DB4xxx	TMMDB4xxx	-

Specific devices not expressly listed in the above table are included in this change.

WHAT IS THE CHANGE?

The current assembly line is moved to the new assembly and test plant in China. The new assembly line will use **same production equipment** with **same assembly flow** and **test process** as the current assembly and test line.

Package	Current	New	
DO-35	Chipa 1	China 2	
MELF / MiniMELF		China 2	

This transfer will have **no impact** on the **assembly materials** and **package construction**. There will be no change in the **dimensional**, **thermal** and **electrical parameters** of the products, maintaining unchanged current information published in the relevant datasheets. All verifications are included in the **qualification program**. The **footprints** recommended by ST for MELF and MiniMELF remain the same.

There is **no change** in the **ECOPACK[®]2 grade**, in the **packing mode** and in the standard **delivery quantities**.

HOW AND WHEN?

Qualification and test results:

The qualification program mainly consists of comparative electrical characterizations and reliability tests. The production ramp-up in the new assembly line will be monitored with a prelaunch control plan implemented on selected parameters.

The **Reliability Report** for the new assembly line qualification will be available in week 04-2012. The Reliability Test Plan is annexed to the present document.

Sampling:

Qualification samples of the devices listed below and produced in the China 2 plant will be available from week 01-2012 on request.

Product Family	Package	Test Vehicle Salestypes
	DO 25	1N5711
	DO-35	BAT46
	MELE	TMBYV10-40FILM
Schottky Diodes		TMBYV10-60FILM
		TMM6263
	MiniMELF	TMMBAT41FILM
		TMMBAT48FILM
	DO-35	DB3
DIACS	MiniMELF	TMMDB3

Other samples will be available on request for delivery upon mass production start.

Change implementation schedule:

The **mass production** and **first shipments** will start according to our work in progress and materials availability as indicated in the schedule below.

Package	Production Start	1st Shipments
DO-35 MELF / MiniMELF	From week 04-12	From week 06-12

Absence of acknowledgement of this PCN within **30 days** of receipt will constitute acceptance of the change. After an acknowledgement, unless otherwise previously agreed to in writing for a specific process change requirement or for device specific requirements, absence of additional response within **90 days** of receipt of this PCN will constitute acceptance of the change. Shipments may in any case start earlier with the customer's written agreement.

Traceability:

The **traceability** of products issued from the new assembly plants will be ensured by an **internal codification** and by the **Q.A. number**.

Annex: Reliability Test Plan for qualification



Reliability test plan for qualification

Glass diodes assembly, test and finishing transfer to a new Chinese plant

General Information		Ī	Locations	
Product Lines	BU 58 and BU 78		Wafer fab	ST TOURS
Products Description	DIAC Signal Schottky diodes		Assembly plant	Chinese subcontractor
Product Group	IMS		Reliability Lab	ST TOURS
Product division	APM		Reliability assessment	To Be Defined
Packages	DO-35, MELF and MiniMELF			
Silicon Process technologies	GLASS			

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	17/10/11	11	S. Jacques	Presentation of the reliability test plan for qualification

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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<u>1</u> APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 22	Reliability test methods for packaged devices
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
MIL-STD-750C	Test method for semiconductor devices
SOP 2610	General product qualification procedure
SOP 2614	Reliability requirements for product qualification

2 GLOSSARY

BOM	Bill Of Materials
D-FMEA	Device-oriented Failure Mode and Effects Analysis
DUT	Device Under Test
F/G	Finished Good
HTS	High Temperature Storage
PCN	Process Change Notification
RH	Relative Humidity
RSH	Resistance to Solder Heat
SAM	Scanning Acoustic Microscopy
SMPS	Switch Mode Power Supply
SS	Sample Size
ТСТ	Temperature Cycling Test
THB	Temperature Humidity Bias



3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

This document deals with the transfer of glass diodes manufacturing (assembly, test and finishing) from an initial Chinese plant (Dongguan) to a new facility, still located in China (Heyuan).

The glass diodes are assembled in DO-35, MELF and MiniMELF packages. These products are dedicated to appliance and SMPS market segments.

It is important to notice that this transfer is performed without any change: same BOM, back-end process and equipments (oven excepted but based on an existing one).

This qualification report is linked to a PCN procedure.

This document describes here the reliability test plan that will be performed soon. This test plan was defined after a D-FMEA procedure following the "stress test driven" method including die and package-oriented tests.

3.2 <u>Conclusion</u>

The reliability test results will be explained later.



<u>4</u> DEVICE CHARACTERISTICS: CONSTRUCTION NOTE

An example of construction note, dedicated to DO-35 and MiniMELF packages, is described below.

Wafer/Die fab. Information	GLASS products
Wafer fab manufacturing location	ST Tours – FRANCE
Technology	GLASS
Die finishing back side	Ti-Ag (e.g. DO-35 package)
Bond pad metallization layers	Ti-Ag (e.g. DO-35 package)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours - FRANCE
Assembly information	
Assembly site	Chinese subcontractor
Package description	DO-35 and MiniMELF
Encapsulation compound	Glass tube
Lead materials	Fe-Ni core recovered with copper
Lead finishing process	Sn
Final testing information	
Testing location	Chinese subcontractor



5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Nine test vehicles were chosen to perform the reliability tests. The part numbers are given below:

- MELF package:
 - TMBYV 10-40: small signal Schottky diode, GLASS silicon die technology. Electrical features: I_{F(AV)} = 1 A, Max. V_F = 0.55 V @ 1 A, V_{RRM} = 40 V.
 - TMBYV 10-60: small signal Schottky diode, GLASS silicon die technology. Electrical features: I_{F(AV)} = 1 A, Max. V_F = 0.7 V @ 1 A, V_{RRM} = 60 V.
- MiniMELF package:
 - TMMBAT41: small signal Schottky diode, GLASS silicon die technology. Electrical features: I_F = 100 mA, Max. V_F = 1 V @ 200 mA, V_{RRM} = 100 V.
 - TMMBAT48: small signal Schottky diode, GLASS silicon die technology. Electrical features: $I_F = 350$ mA, Max. $V_F = 0.9$ V @ 500 mA, $V_{RRM} = 40$ V.
 - $_{\odot}$ TMM6263: small signal Schottky diode, GLASS silicon die technology. Electrical features: I_F = 15 mA, Max. V_F = 1 V @ 15 mA, V_{RRM} = 60 V.
 - ο TMMDB3: DIAC, GLASS silicon die technology. Electrical features: Max. V_{BO} = 36 V, Max. I_{BO} = 50 μA, Max. Leakage current = 10 μA @ 0.5 $V_{BO(max)}$.
- DO-35 package:
 - o 1N5711: small signal Schottky diode, GLASS silicon die technology. Electrical features: $I_F = 15$ mA, Max. $V_F = 1$ V @ 15 mA, $V_{RRM} = 70$ V.
 - o BAT46: small signal Schottky diode, GLASS silicon die technology. Electrical features: $I_F = 150$ mA, Max. $V_F = 1$ V @ 250 mA, $V_{RRM} = 100$ V.
 - ο DB3: DIAC, GLASS silicon die technology. Electrical features: Max. V_{BO} = 36 V, Max. I_{BO} = 50 μA, Max. Leakage current = 10 μA @ 0.5 $V_{BO(max)}$.

The qualification plan is summarized in the following tables.

	MELF p	ackage	MiniMELF package					
	TMBYV 10-40	TMBYV 10-60	TMMBAT41	TMMBAT48	TMM6263	TMMDB3		
Bubble test		Х			Х			
Solderability		Х			Х			
Lead bending								
THB				Х				
TCT		Х			Х	Х		
RSH	Х		Х			Х		
HTS						Х		

	DO-35 package						
	1N5711	BAT46	DB3				
Bubble test	Х						
Solderability	Х						
Lead bending	Х		Х				
THB							
TCT	Х		Х				
RSH		Х	Х				
HTS			Х				



5.2 <u>Test plan and results summary</u>

					Failure/SS	
Test	Std ref.	Conditions	SS	Steps	TMYV10- 40	TMYV10- 60
Hermiticity "Bubble test"	MIL-STD-883E Method 1014-C1	7 bars 2 h	TBD	2 h		TBD
Solderability	MIL-STD-750D Method 2026	- Steam aging (100 ℃, 8 h), SnAgCu bath, 245 ℃ / 3 s - Dry aging (150 ℃, 16 h), SnAgCu bath, 245 ℃ / 3 s - Steam aging (100 ℃, 8 h), SnPb bath, 220 ℃ / 5 s - Dry aging (150 ℃, 16 h), SnPb bath, 220 ℃ / 5 s - Steam aging (100 ℃, 8 h), SnAgCu bath, 260 ℃ / 3 s - Dry aging (150 ℃, 16 h), SnAgCu bath,	TBD	Measurement		TBD
тст	JESD22 A-104	-55 ℃/+150 ℃ 1 cycles/h	TBD	100 cycles		TBD
		500 cycles		500 cycles		TBD
RSH	J-STD-002	260 ℃ 10 s ON 15 s OFF 2 dippings	TBD	Measurement	TBD	

Reliability test results on the devices assembled in a MELF package



•	Reliability	test results or	n the devices	assembled in a	MiniMELF package
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Tost	Std ref	Conditions	22	Stens	Failure/SS	
1631	Test Statel. Collations		55	Steps	TMMBAT41	TMMBAT48
		85 °C		168 h		TBD
ТНВ	JESD22 A-101	85% RH Bias = 100 V	TBD	500 h		TBD
		1000 h		1000 h		TBD
RSH	J-STD-002	260 ℃ 10 s ON 15 s OFF 2 dippings	TBD	Measurement	TBD	

Test	Std ref	Conditions	SS Steps Fa		Failu	re/SS
				Ctope	TMM6263	TMMDB3
Hermiticity "Bubble test"	MIL-STD-883E Method 1014-C1	7 bars 2 h	TBD	2 h	TBD	
Solderability	MIL-STD-750D Method 2026	- Steam aging (100 ℃, 8 h), SnAgCu bath, 245 ℃ / 3 s - Dry aging (150 ℃, 16 h), SnAgCu bath, 245 ℃ / 3 s - Steam aging (100 ℃, 8 h), SnPb bath, 220 ℃ / 5 s - Dry aging (150 ℃, 16 h), SnPb bath, 220 ℃ / 5 s - Steam aging (100 ℃, 8 h), SnAgCu bath, 260 ℃ / 3 s - Dry aging (150 ℃, 16 h), SnAgCu bath,	TBD	Measurement	TBD	
тст	JESD22 A-104	-55 ℃/+150 ℃ 1 cycles/h 500 cycles	твd	100 cycles 500 cycles	TBD TBD	TBD TBD
RSH	J-STD-002	260 ℃ 10 s ON 15 s OFF 2 dippings	TBD	Measurement		TBD
HTS	MIL-STD-750C Method 1032	150 ℃ 1000 h	TBD	1000 h		TBD



•	Reliability test results on the devices assembled in a DO-35 package	je
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Tost	Std ref Conditions S	99	Stons	Failure/SS			
Test	Sturei.	Conditions	55	Steps	1N5711	BAT46	DB3
Hermiticity "Bubble test"	MIL-STD-883E Method 1014-C1	7 bars 2 h	твd	2 h	TBD		
Solderability	MIL-STD-750D Method 2026	- Steam aging (100 ℃, 8 h), SnAgCu bath, 245 ℃ / 3 s - Dry aging (150 ℃, 16 h), SnAgCu bath, 245 ℃ / 3 s - Steam aging (100 ℃, 8 h), SnPb bath, 220 ℃ / 5 s - Dry aging (150 ℃, 16 h), SnPb bath, 220 ℃ / 5 s - Steam aging (100 ℃, 8 h), SnAgCu bath, 260 ℃ / 3 s - Dry aging (150 ℃, 16 h), SnAgCu bath,	TBD	Measurement	TBD		
Leads integrity	Leads bending	Terminals strength and lead bending 1 cycle	TBD	Measurement	TBD		TBD
тот		-55 ℃/+150 ℃	тор	100 cycles			TBD
	JESD22 A-104	1 cycles/h 500 cycles	IBD	500 cycles			TBD
RSH	J-STD-002 J-STD-002 260 °C 10 s ON 15 s OFF 2 dippings	TBD	Measurement		TBD	TBD	
HTS	MIL-STD-750C Method 1032	150 ℃ 1000 h	TBD	1000 h			TBD



<u>6</u> <u>ANNEXES</u>

6.1 <u>Tests Description</u>

Test name	Description	Purpose
Die and Package-oriented test		
HTS High Temperature Storage	The device is stored in unbiased condition at the maximum temperature allowed by the package materials, sometimes higher than the maximum operating temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress- voiding.
RSH Resistance to Solder Heat	The device is submitted to a dipping in a solder bath at $260 \ {\cmu}$ with a dwell time of 10 s.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.
Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.	To provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature, and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cyclic temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure mechanisms are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die- attach layer degradation.



6.2 Drift analysis

In addition to the table of results (refer to item 5), the graphs presented in the next pages will provide a straightforward data analysis with a representation of the selected parameter population in the Henry's chart.

Since the « y » axis represents the cumulative population of the different read-outs, statistical analysis is easy (median, range), while the overall stability and span during the stress test is immediately evident.

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