

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MIC/11/6875 Notification Date 10/20/2011

Qualification of a new wafer fab for STM32F100xxxxB low and medium density devices

Table 1.	Change	Implementation	Schedule
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Forecasted implementation date for change	19-Jan-2012
Forecasted availabillity date of samples for customer	13-Oct-2011
Forecasted date for STMicroelectronics change Qualification Plan results availability	13-Nov-2011
Estimated date of changed product first shipment	19-Jan-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	All STM32F100xxxxB low and medium density devices	
Type of change	Waferfab additional location	
Reason for change	Need for improved production flexibility	
Description of the change	Fab 11 is already qualified for STM32F10x medium/high/low density. This PCN aims to extend this qualification to STM32F100xxxxB low and medium density devices in order to support current and future customer demand and improve ou service through increased capacity and improved manufaturing flexibility. All datasheet parameters are identical to Fab3 silicon.	
Product Line(s) and/or Part Number(s)	See attached	
Description of the Qualification Plan	See attached	
Change Product Identification	Package marking from "93" to "9U"	
Manufacturing Location(s)		

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	PCN MMS-MIC/11/6875
Please sign and return to STMicroelectronics Sales Office	Notification Date 10/20/2011
Qualification Plan Denied	Name:
Qualification Plan Approved	Title:
	Company:
Change Denied	Date:
Change Approved	Signature:
Remark	
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Name	Function	
Colonna, Daniel	Division Marketing Manager	
Buffa, Michel	Division Product Manager	
Narche, Pascal	Division Q.A. Manager	

DOCUMENT APPROVAL



0.18 FLASH TECHNO WF11 SECOND SOURCE QUALIFICATION

CHARACTERISATION PLAN

October 6th 2011,V1.0

STMicroelectronics

WF11 – PRODUCT ELECTRICAL CHARACTERISATION PLAN

Fab electrical parameter of the process between 2 wafer fab = 0 deviation in limit & target
3 products of this family as a reference already qualified and certified without any deviation (ref to characterization report 240510_410_F11.doc)

- ManufacturingTest & Detection : yield & datalog = identical
 - 2 lots
 - 1 corner lot

•Electrical characterization on critical parameters to guarantee datasheet specification

TEST VEHICLE	STM32F100
DIE NAME	420
MEMORY	FLASH 0.18µm / 128KB
EWS site	Ardentec
PACKAGE	LQFP100 14*14
ASSEMBLY SITE	ATK1
FT site	ATK3



WF11 – PRODUCT ELECTRICAL CHARACTERISATION CRITICAL PARAMETERS

Datasheet parameter	Characterization parameter	Characterized Sample
LOW CONSUMPTION STOP Regon	Temperature	Digital transistor Std & Corner lot
ADC (INL,DNL,Offset)	Temperature & power supply	Digital transistor Std lot

Note that critical electrical parameters are yield monitored and datalogged on all lots mentionned





FAB11 SECOND SOURCE QUALIFICATION for STM32 128K VALUE

RELIABILITY PLAN

Oct 4th, 2011 V1.0

STMicroelectronics

FAB11 – 128KB VALUE QUALIFICATION

THE 0.18 FLASH TECHNOLOGY IS QUALIFIED BASED ON 3 LOTS (1) AND IN PRODUCTION. THUS, THESE DATA ALLOW TO PROLIFERATE STM32 128KB VALUE BY PERFORMING RELIABILITY TRIALS WITH ONLY 1 LOT AS SHOWN IN TABLE BELOW :

TEST VEHICLE	STM32F100V8T6B	
DIE NAME	420_1 (revZ)	
MEMORY	FLASH 0.18µm / 128KB	
PACKAGE	LQFP100 14*14	
ASSEMBLY SITE	MALTA	
QUALIFICATION LOTS	1 STD LOT	
QUALIFICATION LOTS	HP132ACS	
RELIABILITY DURATION	4 weeks	

(1) : Qual report RERMCD1022



VALUE QUALIFICATION – RELIABILITY PLAN

TEST	SPECIFICATION	NB OF PARTS	ACCEPTANCE CRITERIA
		LOT 1	
ESD HBM/CDM Latch-up	JEDEC Std JESD22 AEC Q100	ESD : 2 x 3pcs LU : 1 x 5pcs	HBM 2 kV / CDM 500 V LU @ 125°C No reject with std FT
HIGH TEMPERATURE OPERATING LIFE TEST	MIL Std 883E Method 1005	1 x 80pcs	168 HRS / 140℃ / 4V No reject with std FT
HIGH TEMPERATURE RETENTION BAKE AFTER HOT CYCLING	MIL Std 883E Method 1008	1 x 80pcs	72 HRS / 175℃ / No Bias sampl es pre-cycled 10K@125℃ No reject with std FT



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