PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM/11/6872
Notification Date 10/31/2011

MATERIAL SET CHANGE (Cu wire 1.3 mils) for SO-8 package in ST Shenzhen (China) with ECOPAK 2 (Halogen Free) capability

Table 1. Change Implementation Schedule

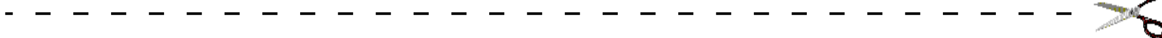
Forecasted implementation date for change	12-Jan-2012
Forecasted availabillity date of samples for customer	24-Oct-2011
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	24-Oct-2011
Estimated date of changed product first shipment	30-Jan-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly material change
Reason for change	To improve service to ST Customers
Description of the change	Progressing on the activities related to quality improvement and along the plan of rationalizing the manufacturing processes, ST is glad to extend for the involved products the wires material from Au to Cu (1.3 mils) and announces the implementation of the Ecopack 2 (also called "Halogen Free") for the SO-8 package in the ST plant of Shenzhen (China).
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	ECOPACK 2 grade identification printed on the inner and external box
Manufacturing Location(s)	1]St Shenzhen -China

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM/11/6872**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 10/31/2011**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
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De marco, Alberto	Division Product Manager
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Bugnard, Jean-Marc	Division Q.A. Manager
Lisi, Giuseppe	Division Q.A. Manager
Motta, Antonino	Division Q.A. Manager

Reliability Evaluation Report

To qualify SOIC8L 1.3mil Cu wire in STS-

T.V.: L4931ABD50-TR$2Z – Line: LW05
and
SUMITOMO EME-G700K

General Information	
Product Line	LW05
Product Description	Very low drop voltage regulators with inhibit
P/N	L4931ABD50-TR$2Z
Product Group	IMS, APM Group
Product division	**Linear Voltage Regulators & Vref** **Mixed Processes Division**
Package	SO8
Silicon Process technology	BIP (>6um)

Locations	
Wafer fab	AMK6 6"
Assembly plant	STS
Reliability Lab	**IMS-APM Catania Reliability Lab**

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	27-Jul-2011	9	Stefania Motta	Giovanni Presti	First Issue

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify SOIC8L 1.3mil Cu wire in STS

On the LW05 line (the smallest die size among the TV) the reliability verification has been performed on corner lots (LL, HH bonding parameters) too.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure) until the final step @ 1000h. Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime..

4 DEVICE CHARACTERISTICS

4.1 Device description

The L4931ABxx L4931Cxx are very Low Drop regulators available in TO-220, SO-8, DPAK, PPAK and TO-92 packages and in a wide range of output voltages.
The very low drop voltage (0.4 V) and the very low quiescent current make them particularly suitable for low noise, low power applications and specially in battery powered systems.
A TTL compatible shutdown logic control function is available in PPAK and SO-8 packages.
This means that when the device is used as a local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. It requires only a 2.2 µF capacitor for stability allowing space and cost saving.

4.2 Construction note

	P/N L4931ABxx
Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6 6"
Technology	BIP (>6um)
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	1770,1850 UM
Bond pad metallization layers	1
Passivation type	SiN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac EWS 0899
Tester	QT200
Test program	LWXXSPXX.CTS vers. W05
Assembly information	
Assembly site	STS (3068)
Package description	SO 08 .15 JEDEC
Molding compound	**SUMITOMO EME-G700K**
Frame material	SO 8L 94x125 MtBt 4+2+2 NiThPdAgAu(5FT07810)
Die attach process	Epoxy
Die attach material	ABLEBOND 8601S-25 10cc/21g Sy EFD(5ST96950)
Die pad size	94x125 mils
Wire bonding process	ASM Eagle60 Thermosonic Bonding
Wires bonding materials/diameters	1.3mil Cu(5XC13779)
Final testing information	
Testing location	STS(3068)
Tester	QT200
Test program	LW2SFH50.CTS

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Package / Moldin Compound	Product Line	Comments
1	**6104HX0**	**GK1121DS**	SO8 / SUMITOMO EME-G700K	LW05	QUALIFIC LOT NN
2	**6047L64**	**GK1041Y2**	SO8 / SUMITOMO EME-G700K	LW05	1st CORNER LOT LL
3	**6047L64**	**GK1041Y2**	SO8 / SUMITOMO EME-G700K	LW05	2nd CORNER LOT HH

5.2 Test plan and results summary

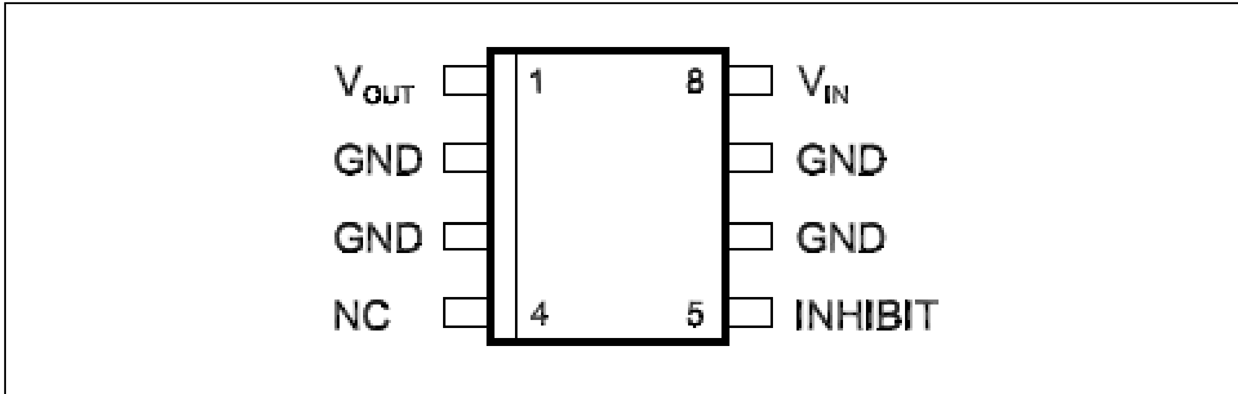
P/N L4931ABD50-TR$2Z

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					note
						Lot 1 LOT NN	Lot 2 LOT LL	Lot 3 LOT HH			
Die Oriented Tests											
HTS	N	JESD22 A-103	Tj = 150℃		168 H	0/45	0/45	0/45			
					500 H	0/45	0/45	0/45			
					1000 H	0/45	0/45	0/45			
HTS	N	JESD22 A-103	Tj = 175℃		168 H	0/45	0/45	0/45			Engineering Evaluation
					500 H	0/45	0/45	0/45			
					1000 H	0/45	0/45	0/45			
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times		Final	Pass	Pass	Pass			
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃		96 H	0/77	0/77	0/77			
					168 H	0/77	0/77	0/77			
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃		100 cy	0/77	0/77	0/77			
					300 cy	0/77	0/77	0/77			
					500 cy	0/77	0/77	0/77			

6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Block diagram

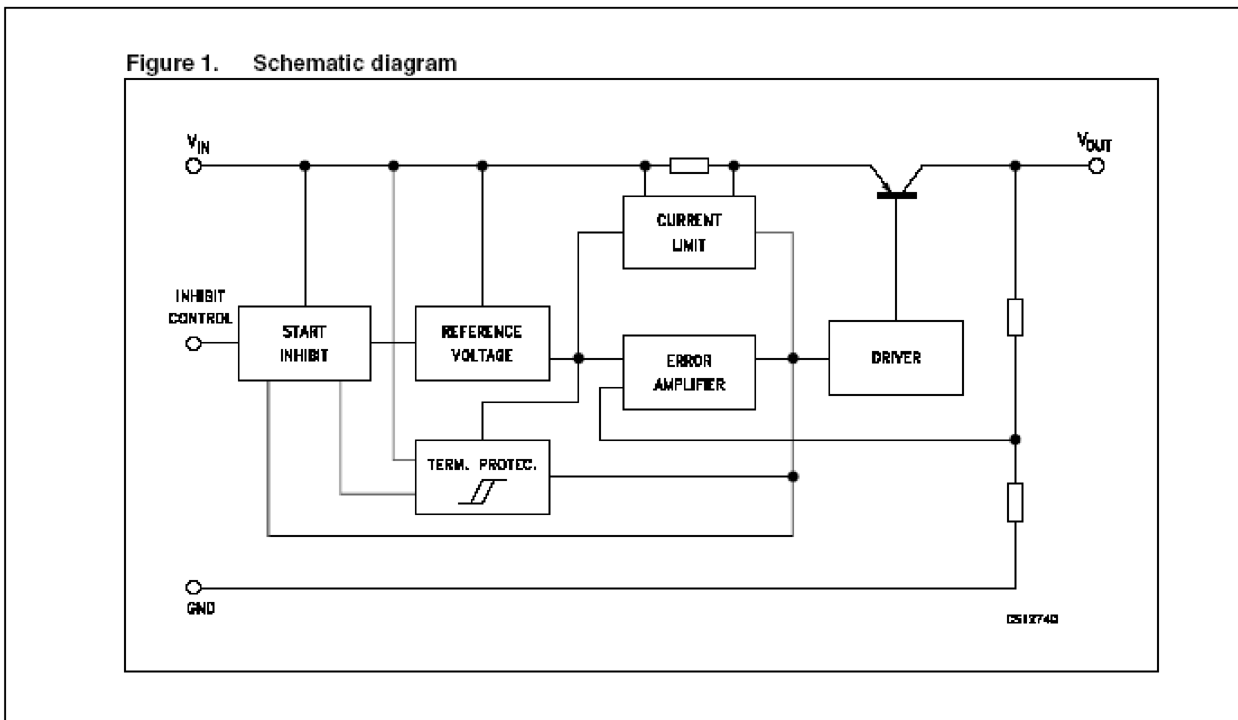
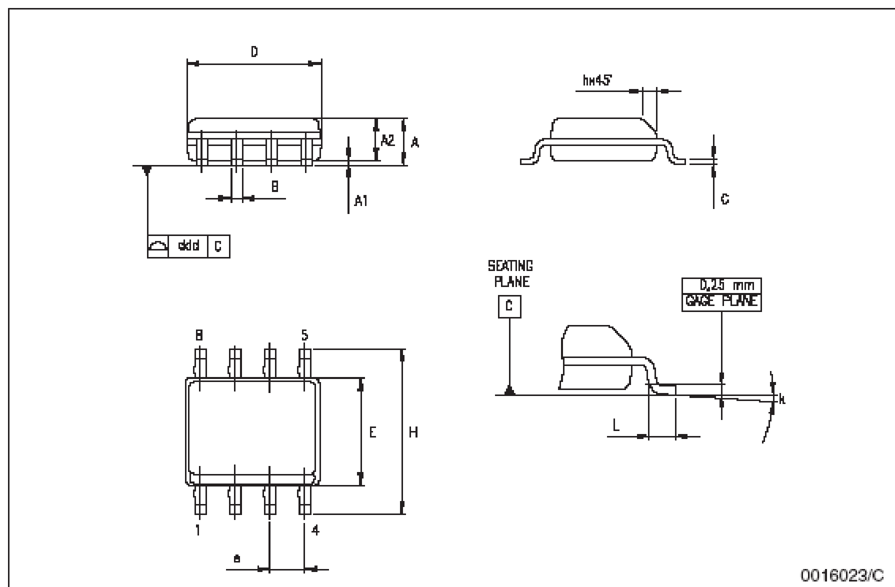


Figure 1. Schematic diagram

6.1.3 Package outline/Mechanical data

SO-8 mechanical data						
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Reliability Report

SO08 1.3 Mils Cu wire
Assy:Shenzhen
TV: ST890CDR – UD91 line
BCD5 Technology

General Information	
Product Line	UD91
Product Description	Power switch with thermal shut down
P/N	ST890CDT
Product Group	APM
Product division	*HiRel & Standard Products*
Package	SO8
Silicon Process technology	BCD5

Locations	
Wafer fab	Agrate
Assembly plant	ST Shenzhen
Reliability Lab	Reliability Lab. Site Catania
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Pages	Prepared by	Approved by	Comment
1.0	9	Giuseppe Failla	Giovanni Presti	First Issue

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Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability Qualification on SO8 1.3 mils Cu wire in ST Shenzhen.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The ST890 is a low voltage, P-channel MOSFET power switch intended for high side load switching applications.
This switch operates with inputs from 2.7 V to 5.5 V, making it ideal for both 3 V and 5 V systems.
Internal current limiting circuitry protects the input supply against overload. Thermal overload protection limits power dissipation and junction temperatures. The ST890B and ST890C's maximum current limits is 1.2 A. The current limit through the switch is programmed with a resistor from SET to ground.
The ST890 is available in SO-8 package.

4.2 Construction note

	P/N ST890CDR
Wafer/Die fab. information	
Wafer fab manufacturing location	Agrate
Technology	BCD5
Process family	BCD
Die finishing back side	Lapped silicon
Die size	2.14x1.83mm
Bond pad metallization layers	AlSiCu
Passivation type	Teos + PTeos + SiOn + PIX
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Shenzhen
Tester	QT200
Test program	UD91F1 00
Assembly information	
Assembly site	ST Shenzhen
Package description	SO8
Molding compound	Sumitomo G700K
Frame material	Copper
Die attach process	epoxy
Die attach material	ABLEBOND 8601S-25
Die pad size	94x125
Wire bonding process	Thermosonic ball bonding
Wires bonding materials/diameters	Copper 1.3 mils
Lead finishing process	preplated
Lead finishing/bump solder material	NiPdAgAu
Substrate supplier for BGA	NA
Final testing information	
Testing location	ST Shenzhen
Tester	QT200
Test program	UD91F1 00

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Process/ Package	Product Line	Comments
1	No info available	GK11813FZZ	SO08	UD91	Final

5.2 Test plan and results summary

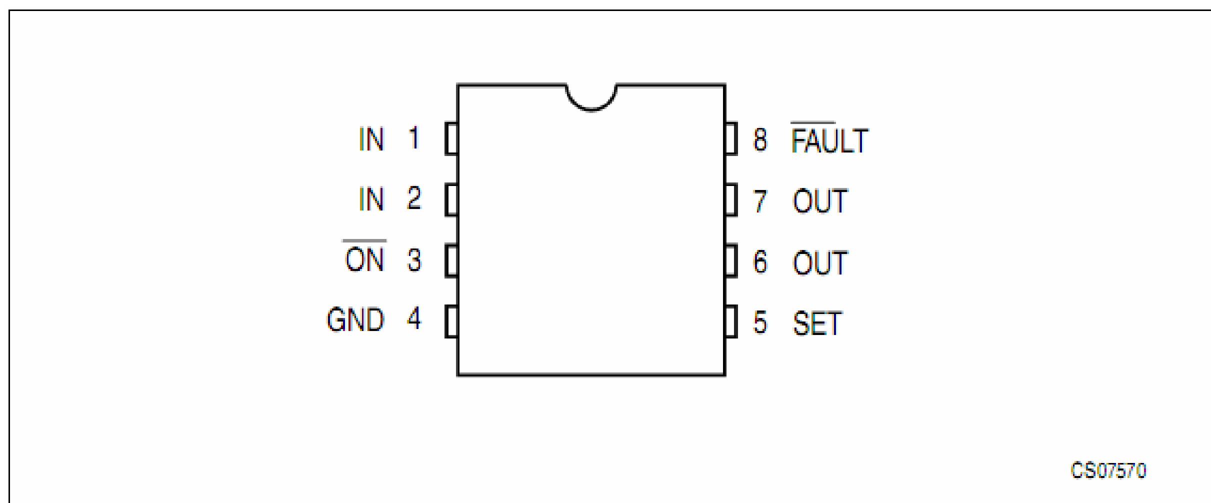
P/N ST890CDR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
Die Oriented Tests							
HTS	N	JESD22 A-103	Ta = 150℃	45	168 h	0/45	
					500 h	0/45	
					1000 h	0/45	
HTS	N	JESD22 A-103	Ta = 175℃	45	168 h	0/45	
					500 h	0/45	
					1000 h	0/45	
HTB	N	JESD22 A-108	Tj = 125℃; Bias=+6V	77	168 h	0/77	
					500 h	0/77	
					1000 h	0/77	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times	250	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	77	168 h	0/77	
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃	77	100 cy	0/77	
					300 cy	0/77	
					500 cy	0/77	
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, Bias=+5V	77	168 h	0/77	
					500 h	0/77	
					1000 h	0/77	

6 ANNEXES

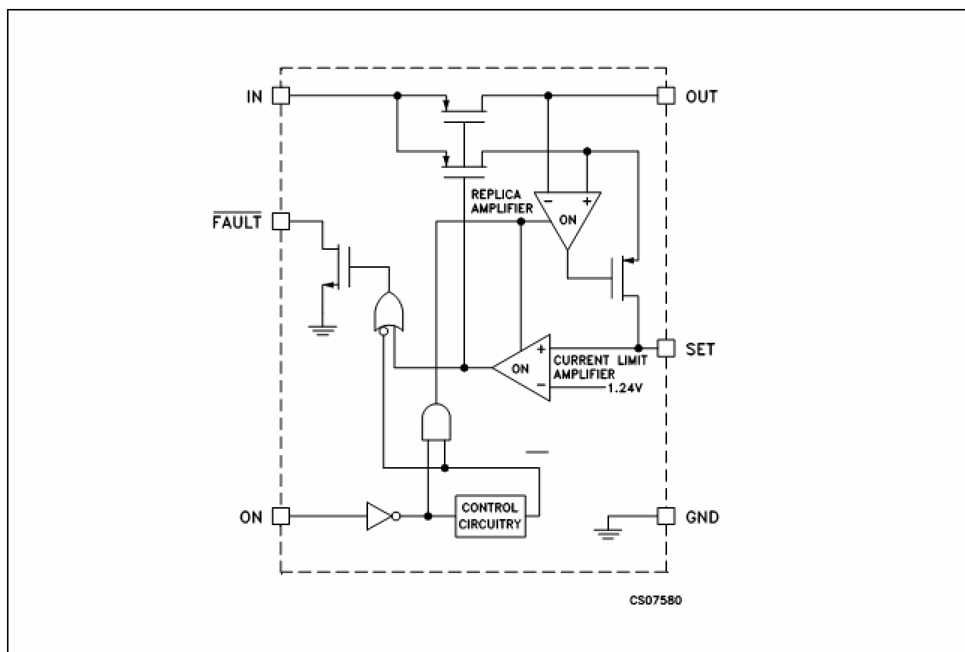
6.1 Device details

6.1.1 Pin connection

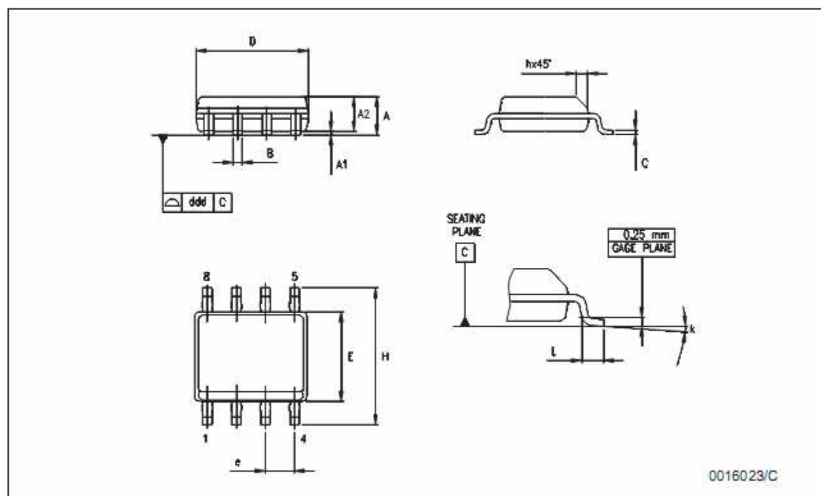


Pin N.	Symbol	Name and function
1, 2	IN	Input P-channel MOSFET source. Bypass IN with a 1 µF capacitor to ground
3	$\overline{ON}$	Active low switch ON input. A logic low turns the switch ON
4	GND	Ground
5	SET	Set current limit input. A resistor from SET to GND sets the current limit for the switch. R_{SET} = 1.38 x 103 / I_{LIM}, where I_{LIM} is the desired current limit in Amperes
6,7	OUT	Switch output. P-channel MOSFET drain. Bypass OUT with a 0.1 µF capacitor to ground
8	$\overline{FAULT}$	Fault indicator output. This open drain output goes low when in current limit or when the die temperature exceeds 135°C

6.1.2 Block diagram



6.1.3 Package outline/Mechanical data



Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8°(max)					
ddd			0.1			0.04

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. Temperature allowed by the package materials, sometimes higher than the max. Operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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