PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM/10/6004
Notification Date 11/04/2010

Conversion to ECOPACK 2 for products housed in: DPAK, IPAK, PPAK, D2PAK, I2PAK and P2PAK packages in the ST plants

Table 1. Change Implementation Schedule

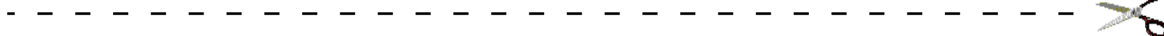
Forecasted implementation date for change	24-Jan-2011
Forecasted availabillity date of samples for customer	28-Oct-2010
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	28-Oct-2010
Estimated date of changed product first shipment	03-Feb-2011

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly material change
Reason for change	To implement massive ECOPACK 2
Description of the change	To move from standard to massive production of ECOPACK 2 graded supply and complete the move to Copper wire bonding. The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets. There is as well no change in the packing process nor in the standard delivery quantities.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	ECOPACK 2 grade identification printed on the inner and external box labels
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM/10/6004**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 11/04/2010**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

....

....

....

....

....

....

....

....

DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Division Marketing Manager
Riviera, Antonio	Division Marketing Manager
Naso, Lorenzo	Division Product Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager
Motta, Antonino	Division Q.A. Manager

Premise

The ECOPACK® program is the cornerstone of our effort of being a leader in the change toward environmentally friendly packaging. In the context of this program, ST develops world class technical solutions designed to progressively remove banned substances from manufacturing.

Continuing in the already announced plan of moving the supply to the ECOPACK®2 grade products (also known in the market as "Halogen Free") and in the aim of a constant process improvement, DPAK, IPAK, PPAK, D²PAK, I²PAK and P²PAK packages will be from now available as ECOPACK®2 graded.

WHY THIS CHANGE?

To implement massive **ECOPACK®2** grade supply DPAK, IPAK, PPAK, D²PAK, I²PAK and P²PAK packages.

This PCN is intended as well, for announcing the completion of the switch for the remaining products using different bonding material, to Copper Wire as communicated by previous CPCN documents DSG-TRA/04/395 and MPA-PWR/06/1963. These packages version, will be entirely manufactured in the ST's premises.

WHAT IS THE CHANGE?

To move from standard to massive production of ECOPACK®2 graded supply and complete the move to Copper wire bonding.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.

There is as well no change in the packing process nor in the standard delivery quantities.

WHEN?

For the products listed in the attached document, the availability will be granted according the following schedule:

Product Family	Package/s	Samples	Full Production
Voltage Regulators	All	Wk 43 (*) '10	Wk 04 ' 11
Power MOSFET	All	Wk 43 (*) '10	Wk 04 ' 11
Power Bipolar & IGBT	All	Wk 43 (*) '10	Wk 04 ' 11

(*) For Test Vehicle – For other samples please contact Marketing

Change implementation schedule:

The conversion to ECOPACK®2 grade, due to the huge quantities are affected by this change, will be not done in a single step but according to Customer requirements and material availability and will initiate from January 2011. During this transition phase, unless specific Customer-related instructions, ST's is willing to ship either the standard or the **ECOPACK®2** grade supply.

Marking and traceability:

Unless otherwise stated by customer specific requirement, ECOPACK®2 grade parts will be identified by the relevant data code and the related ECOPACK®2 grade identification printed on the inner and external box labels.

Qualification Data:

Qualification reports are in the appendix here attached.

Please note that ST Team is doing all the best for providing you full visibility about these announced changes and to minimize any negative impact it may occur.
While our Marketing and Sales teams are available for additional information when required, we are looking forward to your renewed confidence in STMicroelectronics as the strategic partner of your choice.

Reliability Evaluation Report

D²PAK

HF Epoxy Resin

General Information	
Product Line	LUAD
Product Description	RZDJ*LUADFC1
P/N	LD1085D2T-R$2Z
Product Group	APM
Product division	VR
Package	D²PAK
Silicon Process technology	Bipolar

Locations	
Wafer fab	*Singapore*
Assembly plant	*Shenzhen*
Reliability Lab	*Reliability Lab Site Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	23 Feb. 2010	7	Alfio Rao Giuseppe Giacopello	Giovanni Presti	Final

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY 3
3 RELIABILITY EVALUATION OVERVIEW 3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
4 DEVICE CHARACTERISTICS 4
4.1 DEVICE DESCRIPTION 4
4.2 CONSTRUCTION NOTE 4
5 TESTS RESULTS SUMMARY 5
5.1 TEST VEHICLE 5
5.2 TEST PLAN AND RESULTS SUMMARY 5
6 ANNEXES 6
6.1 DEVICE DETAILS 6
6.2 TESTS DESCRIPTION 7

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

D^2PAK qualification using HF Epoxy Resin

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The LD1085xx is a low drop voltage regulator able to provide up to 3 A of output current.
Dropout is guaranteed at a maximum of 1.2 V at the maximum output current, decreasing at lower loads. The LD1085xx is pin to pin compatible with the older 3-terminal adjustable regulators, but has better performances in term of drop and output tolerance.
A 2.85 V output version is suitable for SCSI-2 active termination. Unlike PNP regulators, where a part of the output current is wasted as quiescent current, the LD1085xx quiescent current flows into the load, so increase efficiency. Only a 10 µF minimum capacitor is need for stability.

4.2 Construction note

	P/N LD1085
Wafer/Die fab. information	
Wafer fab manufacturing location	Singapore
Technology	BIPOLAR
Die finishing back side	Cr/Ni/Au
Die size	3.13x2.36mm
Bond pad metallization layers	1
Passivation type	SiN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac EWS
Tester	QT200
Test program	7139629
Assembly information	
Assembly site	STS *Shenzhen*
Package description	D²PAK
Molding compound	HF Epoxy Resin
Frame material	TO263 Dt 40u Ver7 OptF/G selected NiNiP
Die attach process	Soft solder
Die attach material	Pb95.5Ag2.5Sn2 (5XP92057)
Die pad size	5.38x6.48mm
Wire bonding process	Thermosonic Bonding
Wires bonding materials/diameters	2.0mils Cu wire
Lead finishing process	Pure tin plating
Final testing information	
Testing location	STS
Tester	QT200
Test program	7490171

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot		Process/ Package	Product Line	Comments
1	V685002T	GK9310A201		D²PAK	LUAD	

5.2 Test plan and results summary

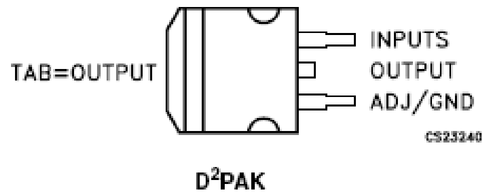
P/N LD1085

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
Die Oriented Tests							
HTSL	N	JESD22 A-103	Ta = 150℃		168 H	0/45	
					500 H	0/45	
					1000 H	0/45	
HTSL	N	JESD22 A-103	Ta = 175℃		168 H	0/45	engineering evaluation
					500 H	0/45	
					1000 H	0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times	160	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃		168 H	0/77	
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃		100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	

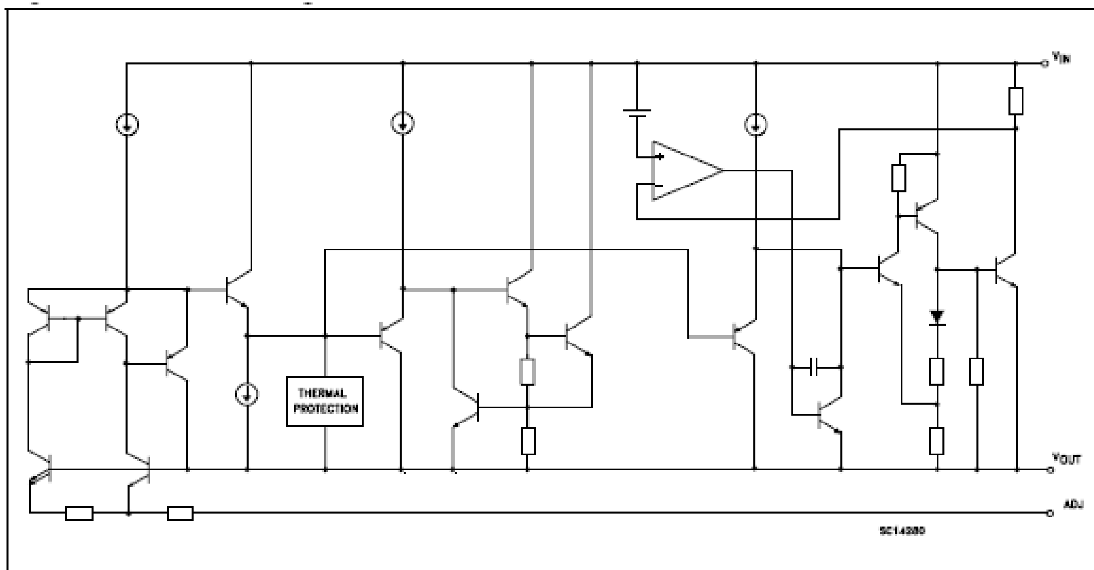
6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Block diagram



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Reliability Evaluation Report

DPAK Package

HF Epoxy Resin

General Information	
Product Line	*LUAD*
Product Description	*3 A low-drop, adjustable positive voltage regulator*
P/N	*LD1085CDT-R*
Product Group	*MSH*
Product division	*IPC*
Package	*DPAK*
Silicon Process technology	*B30II*

Locations	
Wafer fab	Singapore
Assembly plant	*SHENZHEN*
Reliability Lab	*IMS-APM Catania Reliability Lab*
Reliability assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	12-Jul-2010	8	Alfio Riciputo	Giovanni Presti	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY 3
3 RELIABILITY EVALUATION OVERVIEW 3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
3.3 DEVICE DESCRIPTION 4
3.4 CONSTRUCTION NOTE 4
4 TESTS RESULTS SUMMARY 5
4.1 TEST VEHICLE 5
4.2 TEST PLAN AND RESULTS SUMMARY 5
5 ANNEXES 6
5.1 DEVICE DETAILS 6
5.2 TESTS DESCRIPTION 8

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify DPAK package using HF Epoxy Resin.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

3.3 Device description

3 A low-drop, adjustable positive voltage regulator

3.4 Construction note

	LD1085	
	LOT1	LOT2
Wafer/Die fab. information		
Wafer fab manufacturing location	Singapore	
Technology	*B30II*	
Die finishing back side	Cr/Ni/Au	
Die size	3.13x2.36 mm	
Passivation type	SiN	
Wafer Testing (EWS) information		
Electrical testing manufacturing location	APEE Asia Pac EWS 0899	
Tester	QT200	
Test program	LUXXEP**.CTS ver. WAD	
Assembly information		
Assembly site	*SHENZHEN*	
Package description	DPAK	
Molding compound	HF Epoxy Resin	Epoxy resin
Frame material	FRAME TO251 Ve7 OpD SelNi	
Die attach process	Soft solder	
Die attach material	Pb95.5Ag2.5Sn2 (5XP92057)	
Die pad size	3.00 x 4.20 mm	
Wire bonding process	Thermosonic Bonding	
Wires bonding materials/diameters	2.0mils Cu wire	
Lead finishing process	Pure tin plating	
Final testing information		
Testing location	*SHENZHEN*	
Tester	QT200	
Test program	7490171	

4 TESTS RESULTS SUMMARY

4.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line	Comments
1	V60096L7	GK0170KV0B	BZGR*LUADFC1	DPAK	LUAD	Epoxy resin Halogen free
2		GK0170KV0A				Epoxy resin

4.2 Test plan and results summary

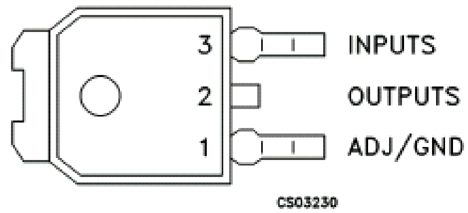
LD1085

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Failure/SS Lot 2	Note
Die Oriented Tests								
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	
					500 H	0/45	0/45	
					1000 H	0/45	0/45	
Package Oriented Tests								
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	
					200 cy	0/77	0/77	
					500 cy	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, Vbias= +24V		168 H	0/77	0/77	
					500 H	0/77	0/77	
					1000 H	0/77	0/77	

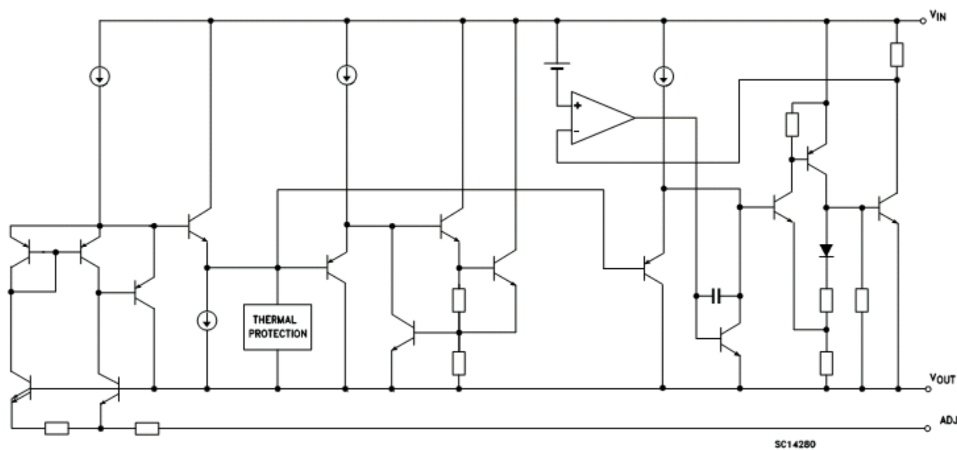
5 ANNEXES

5.1 Device details

5.1.1 Pin connection

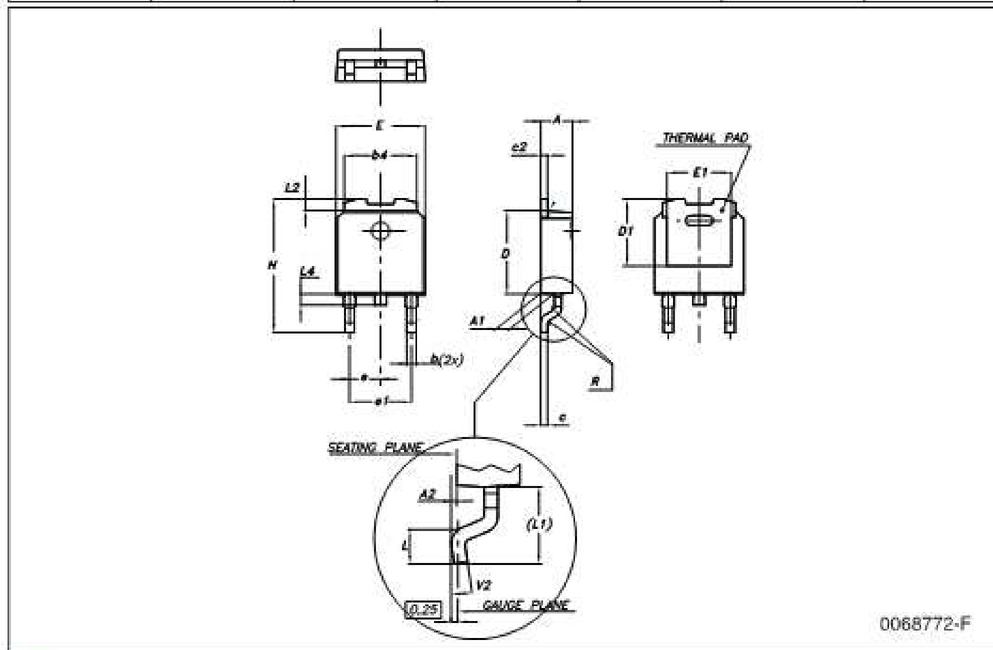


5.1.2 Block diagram



5.1.3 Package outline/Mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



5.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Reliability Evaluation Report

DPAK Package

HF Epoxy Resin

General Information	
Product Line	KSAD
Product Description	RGGR*KSADAA6
P/N	LD1117DTTR
Product Group	APM-MSH
Product division	IPC VR
Package	DPAK
Silicon Process technology	BIPOLAR

Locations	
Wafer fab	Singapore
Assembly plant	*LGG*
Reliability Lab	*IMS-APM* *Catania Reliability Lab*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	12 October 2010	8	Alfio Rao	Giovanni Presti	Final Report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY....3
3 RELIABILITY EVALUATION OVERVIEW....3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
DEVICE CHARACTERISTICS 4
3.3 DEVICE DESCRIPTION....4
3.4 CONSTRUCTION NOTE 4
4 TESTS RESULTS SUMMARY....5
4.1 TEST VEHICLE....5
4.2 TEST PLAN AND RESULTS SUMMARY....5
5 ANNEXES....6
5.1 DEVICE DETAILS....6
5.2 TESTS DESCRIPTION....8

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify DPAK line using Epoxy resin Halogen free.
Test Vehicle: *KSAD - LD1117DTTR*

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. **I**t is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

DEVICE CHARACTERISTICS

3.3 Device description

The LD1117 is a low drop voltage regulator able to provide up to 800 mA of output current, available even in adjustable version (VREF = 1.25 V). Concerning fixed versions, are offered the following output voltages: 1.2 V, 1.8 V, 2.5 V, 2.85 V, 3.0 V, 3.3 V and 5.0 V. The 2.85 V type is ideal for SCSI-2 lines active termination.

3.4 Construction note

	P/N: LD1117DTTR
Wafer/Die fab. information	
Wafer fab manufacturing location	Singapore
Technology	Bipolar
Die finishing back side	Cr/Ni/Au
Die size	1990x1860µm
Passivation type	SiN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac EWS
Tester	QT200
Test program	KSXXEQXX.CTS vers. WAD
Assembly information	
Assembly site	LGG
Package description	DPAK
Molding compound	HF Epoxy Resin
Die attach process	SOLF SOLDER
Die attach material	Pb/Ag/Sn 95.5/2.5/2 D.76mm
Die pad size	3.0x4.2mm
Wire bonding process	Thermosonic Bonding Copper wire
Wires bonding materials/diameters	1.5mils Cu wire
Lead finishing/bump solder material	100% Sn plating
Final testing information	
Testing location	STS
Tester	QT200
Test program	KSX2FAAD.CTS

4 TESTS RESULTS SUMMARY

4.1 Test vehicle

P/N: LD1117DTTR

Lot #	Diffusion Lot	Assy Lot		Process/ Package	Product Line	Comments
1	V6007EE7	KSAD01G		DPAK	KSAD	
2	V6007EE7	KSAD02G				
3	V6004KLJ	KSAD03G				

4.2 Test plan and results summary

P/N: LD1117DTTR

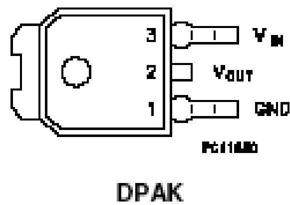
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Failure/SS Lot 2	Failure/SS Lot 3	Note
Die Oriented Tests									
HTB	N	JESD22 A-108	Tj = 125℃, BIAS= +15 V		168 H	0/77	-	-	
					500 H	0/77	-	-	
					1000 H	0/77	-	-	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times		Final	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃		168h	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃		100 cy	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, BIAS= +12 V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	

5 ANNEXES

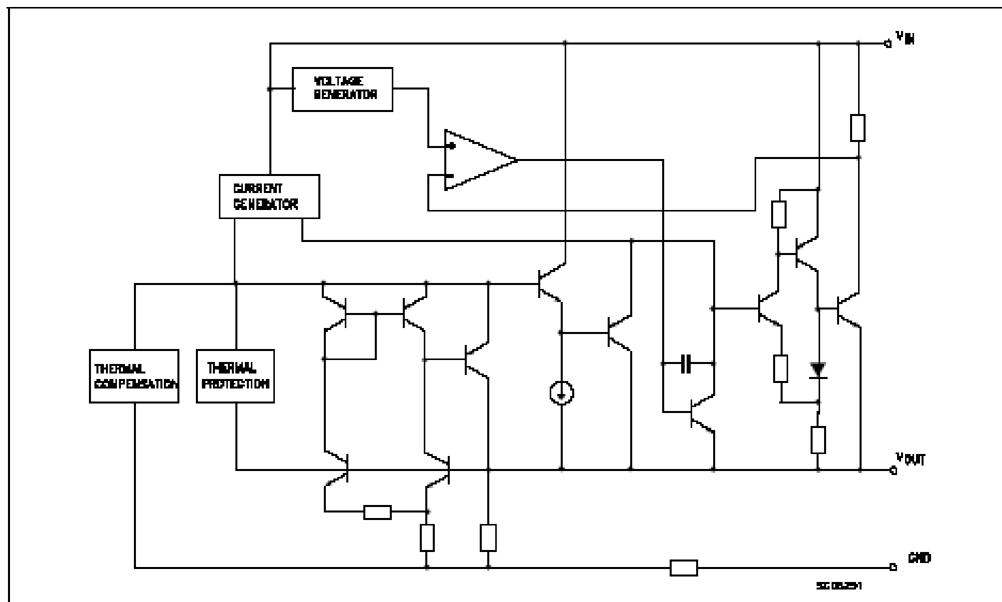
5.1 Device details

5.1.1 Pin connection

Pin connections (top view)

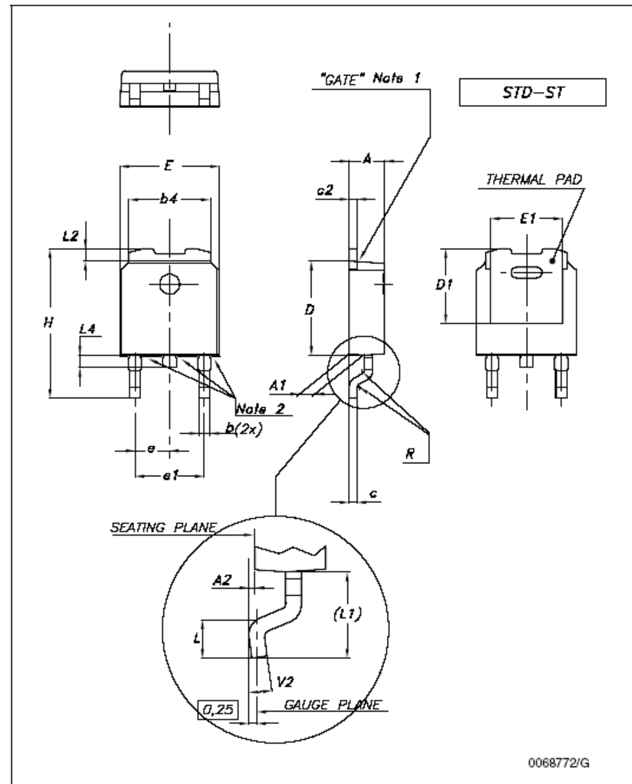


5.1.2 Block diagram



5.1.3 Package outline/Mechanical data

Dim.	Type STD-ST		
	mm.		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°



Note: 1 Maximum resin gate protrusion: 0.5 mm.
2 Maximum resin protrusion: 0.25 mm.

5.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Reliability Report On DPAK package with halogen free resin

General Information	
Product Lines	BA19-B653-3L2S-EL6C-EZ60-EZ62-EZ82
Product Description	N-Channel Power MOSFET NPN Power BIPOLAR
Commercial Products	MJD3055T4 MJD45H11T4 STD20NF06LT4 STD100NH02LT4 STD2HNK60Z STD4NK60ZT4 STD3NK80ZT4
Product Group	IMS – APM
Product division	Power Transistor Division
Package	DPAK
Silicon Process technology	N-Channel Power MOSFET NPN Power BIPOLAR

Locations	
Wafer fab	*BA19 / B653/ EZ82/ EZ60* *Singapore* *EL6C / EZ62 /3L2S* *Catania (ITALY)*
Assembly plant	*LONGGANG (China)* *SHENZHEN (China)*
Reliability Lab	*IMS-APM Catania Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	October-2010	18	G.Montalto G De Luca	G.Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY....3
3 RELIABILITY EVALUATION OVERVIEW....3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
4 DEVICE CHARACTERISTICS....4
4.1 DEVICE DESCRIPTION....4
4.2 CONSTRUCTION NOTE 4
5 TESTS RESULTS SUMMARY....11
5.1 TEST VEHICLE....11
5.2 RELIABILITY TEST PLAN AND RESULTS SUMMARY....11
ANNEXES 6.0....18
6.1TESTS DESCRIPTION 18

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualifications of DPAK package with halogen free resin.

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Power Bipolar, Power MOSFET technology.

4.2 Construction note

D.U.T.: MJD3055T4 LINE: BA19 PACKAGE: DPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	*Singapore*
Technology	Planar NPN Power BIPOLAR
Die finishing back side	AuAs/Cr/Ni/Au
Die size	2240x1940 um
Metal	Al/Si
Passivation type	P-Vapox

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Singapore*
Test program	WPIS

Assembly information	
Assembly site	*LONGGANG (China)*
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Frame coating Ni/NiP
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	7 mils Al Base – 10 mils Al Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*LONGGANG (China)*
Tester	IP TEST

D.U.T.: MJD45H11T4 LINE: B653 PACKAGE: DPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	*Singapore*
Technology	Planar PNP Power BIPOLAR
Die finishing back side	Ti/Ni/Au
Die size	2670x2660 um
Metal	Al/Si
Passivation type	P-Vapox

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Singapore*
Test program	WPIS

Assembly information	
Assembly site	*Shenzhen (China)*
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Frame coating Ni/NiP
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	7 mils Al-Mg Base – 7 mils Al-Mg Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*Shenzhen (China)*
Tester	IP TEST

D.U.T.: STD100NH02LT4 LINE: 3L2S PACKAGE: DPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	*Catania (ITALY)*
Technology	Power MOSFET STripFET Technology
Die finishing back side	Ti/NiV/Au
Die size	3500x2990 um
Metal	AlSiCu
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Catania (ITALY)*
Test program	WPIS

Assembly information	
Assembly site	*Shenzhen (China)*
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Selected Ni/NiP
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag D.76 mm SSD
Wire bonding process	Ultrasonic
Wires bonding materials	15 mils Al Source and 5 mils Al/Mg Gate
Lead finishing/bump solder material	100% Sn

Final testing information	
Testing location	*Shenzhen (China)*
Tester	IP TEST

D.U.T.: STD20NF06LT4 LINE: EL6C PACKAGE: DPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	*Catania (ITALY)*
Technology	Power MOSFET STripFET Technology
Die finishing back side	Ti-Ni-Au
Die size	2550x1950 um
Metal	Al/Si
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Catania (ITALY)*
Test program	WPIS

Assembly information	
Assembly site	*LONGGANG (China)*
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Frame coating Ni/NiP
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate Pad – 10 mils Al Source Pad
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*LONGGANG (China)*
Tester	IP TEST

D.U.T.: STD2HNK60Z LINE: EZ60 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Singapore*
Technology	Power MOSFET SuperMESH Technology
Die finishing back side	Ti-Ni-Au
Die size	2410x2000 um
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Singapore*
Test program	WPIS

Assembly information	
Assembly site	*Shenzhen (China)*
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - selected Ni
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Termosonic
Wires bonding materials	Al
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*Shenzhen (China)*
Tester	IP TEST

D.U.T.: STD4NK60ZT4 LINE: EZ62 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Catania (ITALY)*
Technology	Power MOSFET SuperMESH Technology
Die finishing back side	Ti-Ni-Au
Die size	3180x2650 um
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Catania (ITALY)*
Test program	WPIS

Assembly information	
Assembly site	*LONGGANG (China)*
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Frame coating selected Ni
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Termosonic
Wires bonding materials	2 mils Cu
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*LONGGANG (China)*
Tester	IP TEST

D.U.T.: STD3NK80ZT4 LINE: EZ82 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Singapore*
Technology	Power MOSFET SuperMESH Technology
Die finishing back side	Ti-Ni-Au
Die size	3280x2680 um
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Singapore*
Test program	WPIS

Assembly information	
Assembly site	*LONGGANG (China)*
Package description	*DPAK*
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Frame coating Ni/NiP
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg - 5 mils Al Source Pad
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*LONGGANG (China)*
Tester	IP TEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	MJD3055T4	BA19	Power BIPOLAR
2	MJD45H11T4	B653	Power BIPOLAR
3	STD100NH02LT4	3L2S	Power MOSFET
4	STD20NF06LT4	EL6C	Power MOSFET
5	STD2HNK60Z	EZ60	Power MOSFET
6	STD4NK60ZT4	EZ62	Power MOSFET
7	STD3NK80ZT4	EZ82	Power MOSFET

5.2 Reliability test plan and results summary

D.U.T.: MJD3055T4 LINE: BA19 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die oriented test									
HTRB	N	JEDD22 A-108	T.A.=150°C, Bias 48V	77	168 H	0/77			
					500 H	0/77			
					1000 H	running			
HTSL	N	JESD22 A-103	TA=150°C	77	168 H	0/77			
					500 H	0/77			
					1000 H	running			
Package oriented tests									
PC	-	JESD22-A113-B	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% IR Reflow @ 260°C 3 times		Final	Pass			
AC	N	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77			
TC	Y	JESD22 A-104	TA=-65°C TO +150°C	77	100 cy	0/77			
					200 cy	0/77			
					500 cy	running			
THB	Y	JESD22 A-101	TA=85°C, RH=85% Vbias=50V	77	168 H	0/77			
					500 H	0/77			
					1000 H	running			

D.U.T.: MJD45H11T4 LINE: B653 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die oriented test									
HTRB	N	JEDD22 A-108	T.A.=150℃, Bias 64V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
HTSL	N	JESD22 A-103	TA=150℃	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
Package oriented tests									
PC	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% IR Reflow @ 260℃ 3 times		Final	Pass			
AC	N	JESD22 A-102	Pa=2Atm / Ta=121℃		96 H	0/77			
TC	Y	JESD22 A-104	TA=-65℃ TO +150℃	77	100 cy	0/77			
					200 cy	0/77			
					500 cy	0/77			
THB	Y	JESD22 A-101	TA=85℃, RH=85% Vbias=50V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			

D.U.T.: STD100NH02LT4 LINE: 3L2S PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die oriented test									
HTRB	N	JEDD22 A-108	TA = 175°C, Vbias=16V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
HTFB	N	JEDD22 A-108	Tj=150°C, Vbias=16V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
HTSL	N	JESD22 A-103	TA=175°C	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
Package oriented tests									
PC	-	JESD22-A113-B	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% IR Reflow @ 260°C 3 times		Final	Pass			
AC	N	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77			
TC	Y	JESD22 A-104	TA=-65°C TO +150°C	77	100 cy	0/77			
					200 cy	0/77			
					500 cy	0/77			
THB	Y	JESD22 A-101	TA=85°C, RH=85% Vbias=20V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			

D.U.T.: STD20NF06LT4 LINE: EL6C PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die oriented test									
HTRB	N	JEDD22 A-108	TA = 150℃, Vbias=48V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
HTFB	N	JEDD22 A-108	Tj=150℃, Vbias=20V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
HTSL	N	JESD22 A-103	TA=150℃	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
Package oriented tests									
PC	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% IR Reflow @ 260℃ 3 times		Final	Pass			
AC	N	JESD22 A-102	Pa=2Atm / Ta=121℃		96 H	0/77			
TC	Y	JESD22 A-104	TA=-65℃ TO +150℃	77	100 cy	0/77			
					200 cy	0/77			
					500 cy	Running			
THB	Y	JESD22 A-101	TA=85℃, RH=85% Vbias=50V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			

D.U.T.: STD2HNK60Z LINE: EZ60 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die oriented test									
HTRB	N	JEDD22 A-108	TA = 150℃, Vbias=480V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
HTFB	N	JEDD22 A-108	Tj=150℃, Vbias=30V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
HTSL	N	JESD22 A-103	TA=150℃	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			
Package oriented tests									
PC	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% IR Reflow @ 260℃ 3 times		Final	Pass			
AC	N	JESD22 A-102	Pa=2Atm / Ta=121℃		96 H	0/77			
TC	Y	JESD22 A-104	TA=-65℃ TO +150℃	77	100 cy	0/77			
					200 cy	0/77			
					500 cy	0/77			
THB	Y	JESD22 A-101	TA=85℃, RH=85% Vbias=100V	77	168 H	0/77			
					500 H	0/77			
					1000 H	0/77			

D.U.T.: STD4NK60ZT4 LINE: EZ62 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die oriented test									
HTRB	N	JEDD22 A-108	TA = 150℃, Vbias=480V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
HTFB	N	JEDD22 A-108	Tj=150℃, Vbias=30V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
HTSL	N	JESD22 A-103	TA=150℃	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
Package oriented tests									
PC	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% IR Reflow @ 260℃ 3 times		Final	Pass			
AC	N	JESD22 A-102	Pa=2Atm / Ta=121℃		96 H	0/77			
TC	Y	JESD22 A-104	TA=-65℃ TO +150℃	77	100 cy	0/77			
					200 cy	0/77			
					500 cy	Running			
THB	Y	JESD22 A-101	TA=85℃, RH=85% Vbias=100V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			

D.U.T.: STD3NK80ZT4 LINE: EZ82 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die oriented test									
HTRB	N	JEDD22 A-108	TA = 150°C, Vbias=640V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
HTFB	N	JEDD22 A-108	Tj=150°C, Vbias=30V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
HTSL	N	JESD22 A-103	TA=150°C	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			
Package oriented tests									
PC	-	JESD22-A113-B	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% IR Reflow @ 260°C 3 times		Final	Pass			
AC	N	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77			
TC	Y	JESD22 A-104	TA=-65°C TO +150°C	77	100 cy	0/77			
					200 cy	0/77			
					500 cy	Running			
THB	Y	JESD22 A-101	TA=85°C, RH=85% Vbias=100V	77	168 H	0/77			
					500 H	0/77			
					1000 H	Running			

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(‘‘ST’’) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS ‘‘AUTOMOTIVE GRADE’’ MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

© 2010 STMicroelectronics - All rights reserved.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morroco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com