PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-PWR/10/5981
Notification Date 10/18/2010

AUTOMOTIVE Power Bipolar Production conversion from 5" to 6" wafer size ANG MO KIO (SINGAPORE)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	04-Apr-2011
Forecasted availabillity date of samples for customer	11-Oct-2010
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Oct-2010
Estimated date of changed product first shipment	04-Apr-2011

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab process change
Reason for change	To optimize Power BIPOLAR productivity and ST's Wafer FAB utilization
Description of the change	Following the continuous improvement of our service and in order to rationalize and optimize Power BIPOLAR productivity, this document is announcing the conversion from 5" to 6" wafer size for all AUTOMOTIVE products listed in this PCN, currently manufactured in the ST's Ang Mo Kio (Singapore) wafer FAB. 6" wafer size production, guarantees the same quality and electrical characteristics as the current 5"
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	by traceability code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	**PCN APM-PWR/10/5981**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 10/18/2010**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Division Marketing Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

Dear Customer,

Please be informed that Power BIPOLAR wafers for Automotive products, manufactured in the ST's Ang Mo Kio (Singapore) FAB, actually produced in 5" size, will be converted in 6".

The involved product series and affected packages are listed in the table below:

Product Family Code	Product Family Description	Package	Commercial Product / Series
02	Power BIPOLAR Transistors	All	See attached list

Any other Product related to the above series, manufactured in the ST's Ang Mo Kio (Singapore) FAB, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 41-2010.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Code	Product Family Description	Package	Part Number - Test Vehicle
02	Power BIPOLAR Transistors	All	BU941P BU941ZP STD1802T4-A STT818B-A MJD32CT4-A TIP122-A TIP127-A BDW93C-A

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power BIPOLAR Transistors	From Week 14-2011

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of 6” wafer size, manufactured in ST’s Ang Mo Kio (Singapore) FAB, will be ensured by traceability code.

Sincerely Yours.

Reliability Report

Power Bipolar production lines conversion from

5" to 6" wafer's size

General Information	
Product Lines	B586, B587, BA04, BI01, BI12, BB01, BD01, BB03.
Product Description	Power BIPOLAR
Commercial Products	BU941P, BU941ZP, STD1802T4-A, STT818B-A, MJD32CT4-A, TIP122-A, TIP127-A, BDW93C-A.
Product Group	IMS - APM
Product division	Power Transistor Division
Package	TO-220, TO-247, SOT23-6L, DPAK.
Silicon Process technology	PLANAR

Locations	
Wafer fab	*Ang Mo Kio (SINGAPORE)*
Assembly plant	*TO-220:* SHENZHEN (CHINA); *TO-247:* LONGGANG (CHINA); *SOT23-6L:* CARSEM (MALAYSIA); *TO-252 DPAK:* SHENZHEN (CHINA).
Reliability Lab	*IMS-APM Catania Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Sep-2010	20	G.Montalto G. De Luca	G.Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the 6” wafer’s size for Power Bipolar product in Ang Mo Kio Singapore for Automotive Products.

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

PLANAR Power BIPOLAR

4.2 Construction note

D.U.T.: BU941P LINE: B586 PACKAGE: TO-247

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	Planar High voltage standard NPN
Die finishing back side	Ti-Ni-Au
Die size	4520x5130 μm^2
Metal	Al 6.0 µm
Passivation type	PSG

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	According to WPIS specification

Assembly information	
Assembly site	*LONGGANG (CHINA)*
Package description	TO-247
Molding compound	Epoxy Resin
Frame material	RAW COPPER SelNi/NiP
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 7 mils (Base); Al 15 mils (Emitter)
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*LONGGANG (CHINA)*
Tester	IP-tester

D.U.T.: BU941ZP LINE: B587 PACKAGE: TO-247

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	Planar High voltage standard NPN
Die finishing back side	Ti-Ni-Au
Die size	4560x5560 μm^2
Metal	Al 6.0 µm
Passivation type	PSG

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	According to WPIS specification

Assembly information	
Assembly site	*LONGGANG (CHINA)*
Package description	TO-247
Molding compound	Epoxy Resin
Frame material	RAW COPPER SelNi/NiP
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 7 mils (Base); Al 15 mils (Emitter)
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*LONGGANG (CHINA)*
Tester	IP-tester

D.U.T.: STD1802T4-A LINE: BA04 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR NPN
Die finishing back side	AuAs/Cr/Ni/Au
Die size	1780 x 1770 μm^2
Metal	AlSi
Passivation type	P-VAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	WPIS

Assembly information	
Assembly site	*SHENZHEN (CHINA)*
Package description	DPAK
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Thermosonic
Wires bonding materials	Au 2 mils Base Au 2 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*SHENZHEN (CHINA)*
Tester	IP TEST

D.U.T.: STT818B-A LINE: BI01 PACKAGE: SOT23-6L

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR PNP
Die finishing back side	Au-Cr-Ni-Au
Die size	1780 x 1020 μm^2
Metal	Al/Si
Passivation type	P-VAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	WPIS

Assembly information	
Assembly site	CARSEM (MALAYSIA)
Package description	SOT23 6L
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	EPOXY
Die attach material	Glue
Wire bonding process	Thermosonic
Wires bonding materials	Au 2 mils Base Au 2 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	CARSEM (MALAYSIA)
Tester	IP TEST

D.U.T.: MJD32CT4-A LINE: BI12 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR PNP
Die finishing back side	Au/Cr/Ni/Au
Die size	1340 x 1340 μm^2
Metal	Al/Si
Passivation type	P-VAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	WPIS

Assembly information	
Assembly site	*SHENZHEN (CHINA)*
Package description	DPAK
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Base Al/Mg 5 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*SHENZHEN (CHINA)*
Tester	IP TEST

D.U.T.: TIP122-A LINE: BB01 PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR NPN
Die finishing back side	Ti/Ni/Au
Die size	1830 x 1970 μm^2
Metal	Al/Si
Passivation type	P-VAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	WPIS

Assembly information	
Assembly site	*SHENZHEN*
Package description	TO-220
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Base Al/Mg 7 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*SHENZHEN*
Tester	IP TEST

D.U.T.: TIP127-A LINE: BD01 PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR PNP
Die finishing back side	Ti/Ni/Au
Die size	1830 x 1970 μm^2
Metal	Al/Si
Passivation type	P-VAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	WPIS

Assembly information	
Assembly site	*SHENZHEN)*
Package description	TO-220
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Base Al/Mg 7 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*SHENZHEN*
Tester	IP TEST

D.U.T.: BDW93C-A LINE: BB03 PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR NPN
Die finishing back side	AuAs/Cr/Ni/Au
Die size	2490 x 2220 μm^2
Metal	Al/Si
Passivation type	P-VAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	WPIS

Assembly information	
Assembly site	*SHENZHEN (CHINA)*
Package description	TO-220
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 7 mils Base Al 10 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*SHENZHEN (CHINA)*
Tester	IP TEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	BU941P	B586	Power BIPOLAR
2	BU941ZP	B587	Power BIPOLAR
3	STD1802T4-A	BA04	Power BIPOLAR
4	STT818B-A	BI01	Power BIPOLAR
5	MJD32CT4-A	BI12	Power BIPOLAR
6	TIP122-A	BB01	Power BIPOLAR
7	TIP127-A	BD01	Power BIPOLAR
8	BDW93C-A	BB03	Power BIPOLAR

5.2 Reliability test plan and results summary

D.U.T.: BU941P LINE: B586 PACKAGE: TO-247

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=560V	77	1000H	0/77
THB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=100V	77	1000H	0/77
TC	N	JESD22 A-104	TA=-55℃ TO 150℃ (1 HOUR/CYCLE)	77	1000 cy	0/77
TF	N	Mil-Std 750D Method 037	∆TC= 70℃ - Pd=24W	20	10Kcy.	0/20
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

D.U.T.: BU941ZP LINE: B587 PACKAGE: TO-247

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=560V	77	1000H	0/77
THB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=100V	77	1000H	0/77
TC	N	JESD22 A-104	TA=-55℃ TO 150℃ (1 HOUR/CYCLE)	77	1000 cy	0/77
TF	N	Mil-Std 750D Method 037	∆TC= 70℃ - Pd=24W	20	10Kcy.	0/20
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

D.U.T.: STD1802T4-A LINE: BA04 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=80V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=50V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-55℃ TO 150℃ (1 HOUR/CYCLE)	77	1000 cy	0/77
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77
TF	N	Mil-Std 750D Method 037	ΔTC=105℃ - Pd=2W	20	10Kcy.	0/20

D.U.T.: STT818B-A LINE: BI01 PACKAGE: SOT23-6L

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 260°C 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTRB	N	JESD22 A-108	T.A.=150°C Vdd=80V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdd=50V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-55°C TO 150°C (1 HOUR/CYCLE)	77	1000 cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

D.U.T.: MJD32CT4-A LINE: BI12 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125°C STORE 168H @ TA=85°C RH=85% Reflow @ 260°C 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTRB	N	JESD22 A-108	T.A.=150°C Vdd=80V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdd=50V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-55°C TO 150°C (1 HOUR/CYCLE)	77	1000 cy	0/77
AC	N	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77
TF	N	Mil-Std 750D Method 037	ΔTC=105°C - Pd=2W	20	10Kcy.	0/20

D.U.T.: TIP122-A LINE: BB01 PACKAGE: TO-220

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=-80V	77	1000H	0/77
THB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=100V	77	1000H	0/77
TC	N	JESD22 A-104	TA=-55℃ TO 150℃ (1 HOUR/CYCLE)	77	1000 cy	0/77
TF	N	Mil-Std 750D Method 037	ΔTC=105℃ - Pd=4.75W	20	10Kcy.	0/20
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

D.U.T.: TIP127-A LINE: BD01 PACKAGE: TO-220

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=80V	77	1000H	0/77
THB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=50V	77	1000H	0/77
TC	N	JESD22 A-104	TA=-55℃ TO 150℃ (1 HOUR/CYCLE)	77	1000 cy	0/77
TF	N	Mil-Std 750D Method 037	ΔTC=105℃ - Pd=4.75W	20	10Kcy.	0/20
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

D.U.T.: BDW93C-A LINE: BB03 PACKAGE: TO-220

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=80V	77	1000H	0/77
THB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=50V	77	1000H	0/77
TC	N	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
TF	N	Mil-Std 750D Method 037	ΔTC=105℃ - Pd=4.75W	20	10Kcy.	0/20
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF Thermal Fatigue	This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress).	The purpose of this test is to detect assembly defects: improper die-attach, bonding weakness and thermal mismatch among various components of the package.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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