

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-IPC/10/5917 Notification Date 09/27/2010

High Density Matrix Leadframe in Carsem Malaysia for Voltage Reference Products housed in SOT-23 and SOT-323 (3/5/6 leads) packages

Table 1.	Change	Implementation	Schedule
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Forecasted implementation date for change	12-Dec-2010
Forecasted availabillity date of samples for customer	20-Sep-2010
Forecasted date for STMicroelectronics change Qualification Plan results availability	20-Sep-2010
Estimated date of changed product first shipment	27-Dec-2010

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	Voltage Reference Products (see attached list)
Type of change	Package assembly material change
Reason for change	improve service to ST Customers
Description of the change	To respond the ever increasing demand for the products housed in the SOT-23 and SOT-323 3/5/6 leads package types, ST announces the expansion of its manufacturing capacity in the Malaysia factory by the introduction of high density matrix leadframe of 75x240mm size in re-placement of the standard 56x229 mm Dual/Matrix
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	by QA Number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	PCN APM-IPC/10/5917
Please sign and return to STMicroelectronics Sales Office	Notification Date 09/27/2010
Qualification Plan Denied	Name:
Qualification Plan Approved	Title:
	Company:
🗖 Change Denied	Date:
Change Approved	Signature:
Remark	

Name	Function
Riviera, Antonio	Division Marketing Manager
Naso, Lorenzo	Division Product Manager
Motta, Antonino	Division Q.A. Manager

DOCUMENT APPROVAL

WHAT:

To respond the ever increasing demand for the products housed in the SOT-23 and SOT-323 3/5/6 leads package types, ST announces the expansion of its manufacturing capacity in the Malaysia factory by the introduction of high density matrix leadframe of 75x240mm size in replacement of the standard 56x229 mm Dual/Matrix (see below).



Current 56x229mm Dual/Matrix Leadframe

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New high density matrix 75x240mm Leadframe

At the same time, will be implemented the Ecopack2 (also called Halogen Free), here below the list of material:

Material	Current Process	Modified Process
Die attach	ABLEBOND 84-1LMISR4	Loctite QMI519
	Or ABLEBOND 8006NS	or ABLEBOND 8006NS
	(or eutectic for SMDB3)	
Wire	Gold 1 Mils	Gold 1 mils
Leadframe	Copper or Alloy42	HDLF* Copper with same internal layout
Molding compound	Nitto MP8000 or Hitachi	Hitachi CEL-8240 halogen free
	CEL-9220 (halogen free)	
Lead finishing	Matte Sn	NiPdAu or Matte Sn (Protection & IPAD)

For the complete list of the part numbers affected by the change, please refer to the attached Products list.

Samples of test vehicles are available right now for immediate customer qualification.

WHY:

This manufacturing change will improve service to ST Customers, standardize processes for the affected packages and enhance the use of the leading-edge packing and testing facility at the Malaysia subcontractor plant.

HOW:

The qualification program mainly consists of reliability tests and comparative electrical characterizations.

The related reliability report is annexed to this document.

The changes here reported do not affect the electrical, dimensional and thermal parameters of the products, keeping unchanged all information reported on the relevant datasheets.

WHEN:

Te implementation will be finalized within Week 51-10

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by the Q.A. number.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets. There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.



REL.6043-283W-10

Linear Voltage Regulators & Vref Quality and Reliability

Reliability Report

High Density Frame Qualification (Frame: 5FT4248* L/F HDLF matrix SOT23.3L Copper 0.640 x 0.0380)

TS2431 – U782 line Technology BCD2S AMK6 SOT23-3L

Voltage References

General Information			Locations		
Product Line	U782AE6		Wafer fab	AMK6	
Product Description	programmable shunt voltage reference: Adjustable output voltage 2.5 to 24V		Assembly plant	Carsem	
P/N	TS2431		Dellability Lab	CATANUA	
Product Group	IMS-APM		Reliability Lab	CATANIA	
Product division	Linear Voltage Regulators & Vref		Reliability assessment	Pass	
Package	SOT23-3L				
Silicon Process technology	A7 BCD2S				
Production mask set rev.	Rev. C U782A				
Raw Line	AYWX*U782AE6				

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	08-Sep-2010	8	Giuseppe Failla Angelo Basile	Giovanni Presti	Final report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.



REL.6043-283W-10

Linear Voltage Regulators & Vref Quality and Reliability

TABLE OF CONTENTS

1	APPLICABLE AND REFERENCE DOCUMENTS	3
2	GLOSSARY	3
3	RELIABILITY EVALUATION OVERVIEW.	3
-	3.1 OBJECTIVES	3
	3.2 CONCLUSION	3
4	DEVICE CHARACTERISTICS	4
	4.1 DEVICE DESCRIPTION	4
	4.2 CONSTRUCTION NOTE	4
5	TESTS RESULTS SUMMARY	5
	5.1 TEST VEHICLE	5
	5.2 TEST PLAN AND RESULTS SUMMARY	5
6	ANNEXES	6
	6.1 DEVICE DETAILS	6
	6.2 TESTS DESCRIPTION	8



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<u>1</u> APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
AEQ100	Stress test qualification for automotive grade integrated circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

<u>3 RELIABILITY EVALUATION OVERVIEW</u>

3.1 Objectives

To Qualify the U782AE6 line using the high density frame 5FT4248* L/F HDLF matrix SOT23.3L Copper 0.640 x 0.0380.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



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4 DEVICE CHARACTERISTICS

4.1 Device description

The TS2431 is a programmable shunt voltage reference with guaranteed temperature stability over the entire temperature range of operation (-40 to +105 $^{\circ}$ C). The output voltage may be set to any value between 2.5V and 24V with an external resistor bridge. Available in SOT23-3 surface mount package, it can be designed in applications where space saving is a critical issue.

4.2 Construction note

	P/N TS2431			
Wafer/Die fab. information				
Wafer fab manufacturing location	АМК6			
Technology	BCD2S			
Process family	BCD2ASDM-E			
Die finishing back side	Lapped Silicon			
Die size	1420 x760um			
Passivation type	PVAPOX/NITRIDE			
Wafer Testing (EWS) information				
Electrical testing manufacturing location	ТРҮ			
Tester	ASL1000			
Test program	TU782AW.PRG			
Assembly information				
Assembly site	Carsem			
Package description	SOT23-3L			
Molding compound	CEL8240HF10LXC			
Frame material	SOT23H-3L-064038-C194FH			
Die attach process	GLUE			
Die attach material	QMI519			
Wire bonding process	Ball on pads, stick on leads			
Wires bonding materials/diameters	1 mils Au			
Lead finishing process	Plating			
Lead finishing/bump solder material	100% Tin Plate			
Final testing information				
Testing location	M5-EWS			
Tester	Catalyst TE07			
Test program	UQ81FA01			



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5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Lot	Process/ Package	Product Line	Comments
1	ENG2989A	SOT23-3L	U782AE6	High Density Frame

5.2 Test plan and results summary

P/N TS2431

Test PC		Std rof	Conditions	22	SS Steps	Failure/SS	Note
1031				00		Lot 1	
Die Orie	nted	Tests					
					168 H	0/77	
HTB	Ν	A-108	Ta = 125℃, BIAS +6.1V	77	500 H	0/77	
		77 100			1000 H	0/77	
IESD22		JESD22			168 H	0/45	
HTSL	Ν	A-103	Ta = 150℃	45	500 H	0/45	
A-103		77 100			1000 H	0/45	
Package	Ori	ented Tests			-		-
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times		Final	Pass	
AC	Y	JESD22	JESD22 Pa-24tm / Ta-1219		96 H	0/77	
70	A-102		1 d=2Aiii / 1d=1210		168 H	0/77	
					100 cy	0/77	
TC Y	Y	Δ-104	Ta = -65℃ to 150℃	77	200 cy	0/77	
		77 10-1			500 cy	0/77	
					168 H	0/77	
THB	Y	A-101	Ta = 85℃, RH = 85%, BIAS +5V	77	500 H	0/77	
		,			1000 H	0/77	



Linear Voltage Regulators & Vref Quality and Reliability REL.6043-283W-10

6 ANNEXES

6.1 Device details

6.1.1 Pin connection



PIN CONNECTIONS (top view)

6.1.2 Block diagram

Block Diagram





REL.6043-283W-10

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6.1.3 Package outline/Mechanical data

PACKAGE MECHANICAL DATA 3 PINS - TINY PACKAGE (SOT-23)



-	Millimeters			Inches			
Dimensions	Min.	Тур.	Max.	Min.	Тур.	Max.	
A	0.890		1.120	0.035		0.044	
A1	0.010		0.100	0.0004		0.004	
A2	0.880	0.950	1.020		0.037	0.040	
b	0.300		0.500	0.012		0.020	
c	0.080		0.200	0.003		0.008	
D	2.800	2.900	3.040	0.110	0.114	0.120	
E	2.100		2.640	0.083		0.104	
E1	1.200	1.300	1.400	0.047	0.051	0.055	
е		0.950			0.037		
e1		1.900			0.075		
L	0.400	0.500	0.600	0.016	0.020	0.024	
L1		0.540			0.021		
k	0*		8*				



Linear Voltage Regulators & Vref Quality and Reliability

6.2 Tests Description

Test name	Description	Purpose					
Die Oriented							
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.					
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	t To investigate the failure mechanisms activated by high temperature, typically wire-bonds solde joint ageing, data retention faults, metal stress voiding.					
Package Oriented							
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.					
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.					
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.					
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.					

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