PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/10/5902
Notification Date 09/17/2010

M24C64, 64Kbit Serial I2C Bus EEPROM, Redesign and upgrade to the CMOSF8H process technology

Table 1. Change Implementation Schedule

Forecasted implementation date for change	10-Sep-2010
Forecasted availabillity date of samples for customer	10-Sep-2010
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	10-Sep-2010
Estimated date of changed product first shipment	17-Dec-2010

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M24C64
Type of change	Waferfab technology change
Reason for change	Line up to state of art of design
Description of the change	Redesign and upgrade to the new CMOSF8H process technology.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process technology identifier is "K" for CMOSF8H device version
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	**PCN MMS-MMY/10/5902**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 09/17/2010**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
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Malbranche, Jean-Luc	Division Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

M24C64, 64Kbit Serial I2C Bus EEPROM
Redesign and upgrade to the CMOSF8H process technology

What is the change?

The **M24C64**, 64Kbit Serial I²C Bus EEPROM product family, currently produced using the CMOSF6DP26% process technology at the GLOBALFOUNDRIES subcontractor (Singapore) and ST Ang Mo Kio (Singapore) wafer diffusion plants, has been **redesigned** and will be **upgraded** to the **CMOSF8H** process technology at **ST Rousset 8" wafer diffusion plant**.

Following parameters are updated in the revised datasheet (rev. 19 - September 2010):

- Tclqv(min) = 100ns (AC characteristics at 1 MHz, 400kHz or 100 kHz)
- tNS = 80ns (AC characteristics at 1 MHz, 400kHz or 100 kHz)
- ESD HBM passes 3000V

The new M24C64 device offers an ECC (error correction code) logic improving the Read reliability. Seen from the I²C bus, this ECC function is transparent and, internally, writing a single byte is also re-writing contiguous bytes. All details are offered in the ECC paragraph of the M24C64 datasheet (rev. 19).

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24C64 in the new CMOSF8H process technology will increase the production capacity throughput and consequently improve the service to our customers.

Also, new M24C64 devices can be accessed with a 1MHz clock (was 400kHz max for the current CMOSF6DP26% version), that is in "Fast-mode Plus", as defined by the I2C-bus specification.

When?

The production of the upgraded M24C64 with the new CMOSF8H will ramp up from October 2010 and shipments can start from December 2010 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the M24C64 will be qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

The CMOSF8H process technology is already qualified on the M24256 & M24512 product families.

The intermediate **Qualification Report QREE0920** is available and included inside this document.

What is the impact of the change?

- Form: marking change (see **Device marking** paragraph)

- Fit: no change

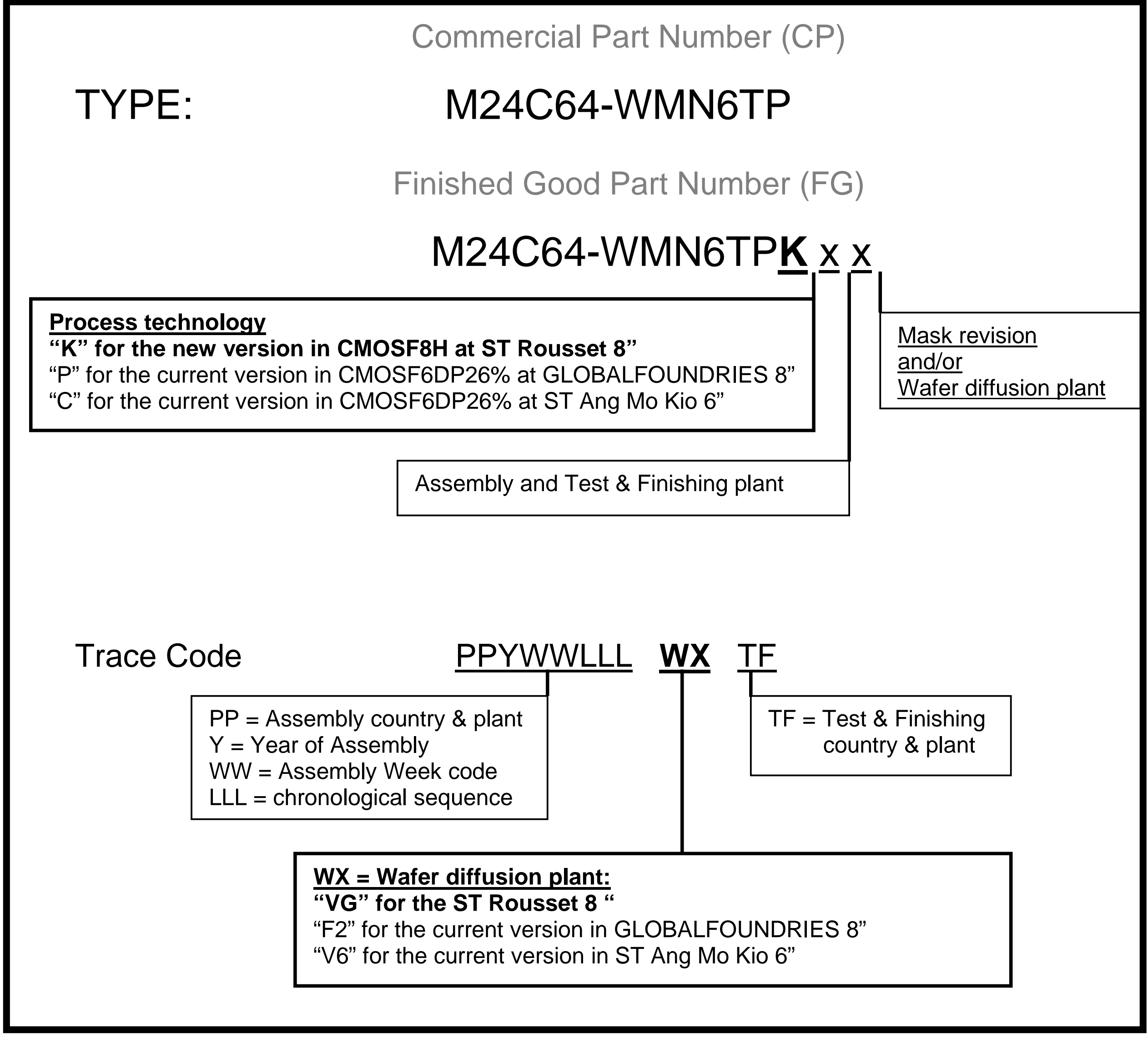
- Function: change on **AC performances** and **ESD HBM** (updated in datasheet **rev. 19**)

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is “**K**” for the **upgraded version** in **CMOSF8H** at the **ST Rousset 8” wafer fab**, this identifier being “P” for the current version in CMOSF6DP26% at the GLOBALFOUNDRIES subcontractor 8” wafer fab and “C” at the ST Ang Mo Kio 6” wafer fab.

➔ *Example for M24C64-WMN6TP (2.5V to 5.5V Vcc range, SO8N – ECOPACK® 2* compliant package)*
** ECOPACK® 2: New grade introduced to identify commonly called “Halogen-Free” products on the market. This grade is also RoHS compliant. (ECOPACK® is a registered trademark of STMicroelectronics)*



How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit "T" for **process technology** identifier is "**K**" for the **upgraded version** in **CMOSF8H** at ST Rousset 8" wafer fab, this identifier being "P" for the current version in CMOSF6DP26% at the GLOBALFOUNDRIES subcontractor 8" wafer fab and "C" at the ST Ang Mo Kio 6" wafer fab.

	Upgraded M24C64 CMOSF8H ST Rousset	Current M24C64 CMOSF6DP GLOBALFOUNDRIES	Current M24C64 CMOSF6DP ST Ang Mo Kio
SO8N Example: M24C64-WMN6TP	24C64WP ST PYWW**K**	24C64WP ST PYWW**P**	24C64WP ST PYWW**C**

For **TSSOP8**, the difference is visible inside the product name: **upgraded version** in **CMOSF8H** is ending by "**K**", the current versions were ending by "P".

	Upgraded M24C64 CMOSF8H	Current M24C64 CMOSF6DP
TSSOP8 Example: M24C64-RDW6TP	464R**K** ST PYWW	464R**P** ST PYWW

P = Assembly plant / country
Y = Last digit of the Year of Assembly
WW = Assembly Week code
T = Process technology code/ Wafer Fab ID

Appendix A- Product Change Information

Product family / Commercial products:	M24C64 products family
Customer(s):	All
Type of change:	Wafer fab Process technology change
Reason for the change:	Line up to state of art of design.
Description of the change:	Redesign and upgrade to the new CMOSF8H Process technology.
Forecast date of the change: (Notification to customer)	Week 36 / 2010
Forecast date of Qualification samples availability for customer(s):	Available
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The intermediate **Qualification Report QREE0920** is available and included inside this document.
Marking to identify the changed product:	Process and fab ID see marking above
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 49 / 2010

Appendix B: Concerned Commercial Part Numbers:

M24C64-RDW6TP
M24C64-RMN6TP
M24C64-WDW6TP
M24C64-WMN6TP

(Related tube versions are also concerned)

Appendix C: Intermediate Qualification Report:

QREE0920
Qualification report

New design / M24C64
using the CMOSF8H technology in the Rousset 8" Fab

Table 1. Product information

General information	
Commercial product	M24C64-RMN6TP M24C64-RDW6TP M24C64-WMN6TP M24C64-WDW6TP M24C64-FDW6TP M24C64-FMC6TG M24C64-FCS6TP/K
Product description	64 Kbit serial I²C bus EEPROM
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8", France
Electrical Wafer Sort test plant location	ST Rousset, France

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor P1, Philippines	Subcon Amkor P3, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor P1, Philippines	Subcon Amkor P3, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcon Amkor P3, Philippines	Subcon Amkor P3, Philippines
WLCSP	Subcon Stats ChipPac, Singapore	Subcon Stats ChipPac, Singapore

Reliability / Qualification assessment: 504 hrs PASS on 2 lots - Pending reliability results 1008 hrs

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M24C64 using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M24C64-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M24C64-R devices
- 1.7 to 5.5 V at –40 to 85 °C for M24C64-F devices

The CMOSF8H is a new advanced silicon process technology that has already been qualified in the ST Rousset 8" fab, and is in production for M24512/M95512 and M24256 EEPROM products. This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

1.2 Conclusion

The new design M24C64 using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab has passed all ESD and latch-up requirements. Product validation and reliability trials are ongoing.

Refer to *Section 3: Reliability test results* for details.

2 Device characteristics

Device description

The M24C64-W, M24C64-R and M24C64-F devices are I2C-compatible electrically erasable programmable memories (EEPROM). They are organized as 8192 × 8 bits.

I2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I2C bus definition.

The device behaves as a slave in the I2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24C64	CMOSF8H	ST Rousset 8"	CDIP8	Engi assy (1)

1. CDIP8 is a ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicle and silicon process technologies used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95512 / M24256 (1)	CMOSF8H	ST Rousset 8"	SO8N	ST Shenzhen
				subcon Amkor P1
			TSSOP8	ST Shenzhen
				subcon Amkor P1
M24C64	CMOSF8H	ST Rousset 8"	UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba
				subcon Amkor P3
			WLCSP	subcon Stats ChipPac

1. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95512/M24256 are applicable.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen & subcon Amkor P1 package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen & subcon Amkor P1 package-oriented tests
- Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24C64 Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	504 hrs	0/80	0/80	Results W39'10
					1008 hrs	Results W38'10	Results W39'10	Results W43'10
	Data retention after endurance							
	AEC-Q100-005	1Million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	504 hrs	0/80	0/80	Results W39'10
					1008 hrs	Results W38'10	Results W39'10	Results W43'10
LTOL	Low temperature operating life							
	JESD22-A108	−40 °C, 6 V	80	3	504 hrs	0/80	0/80	Results W39'10
					1008 hrs	Results W38'10	Results W39'10	Results W43'10
HTSL	High temperature storage life							
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	3	504 hrs	0/80	0/80	Results W39'10
					1008 hrs	Results W38'10	Results W39'10	Results W43'10
WEB	Program/erase endurance cycling + bake							
	Internal spec.	1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 Million cycles / 48 hrs	0/80 (2)	0/80 (2)	Results W39'10
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	3	N/A	Pass > 3000 V	Pass > 3000 V	Pass > 3000 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	6	3	N/A	Pass > 300 V	Pass > 300 V	Pass > 300 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	3	N/A	Class II - Level A	Class II - Level A	Class II - Level A

1. See Table 8: List of terms for a definition of abbreviations.
2. First rejects after 10 million E/W cycles.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen & subcon Amkor P1) (1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M95512		
						Lot1	Lot2	Lot3
PC	Preconditioning: moisture sensitivity level 1							
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345
THB (2)	Temperature humidity bias							
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80
TC (2)	Temperature cycling							
	AEC-Q100-JESD22-A104	−65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80
TMSK (2)	Thermal shocks							
	JESD22-A106	−55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25
AC (2)	Autoclave (pressure pot)							
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80
HTSL (2)	High temperature storage life							
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
ELFR	Early life failure rate							
	AEC-Q100-008	HTOL 150 °C, 6 V	800	3	48 hrs	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)							
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-

1. See Table 8: List of terms for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen & subcon Amkor P1) [(1)]

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95512		
						Lot1	Lot2	Lot3
PC	Preconditioning: moisture sensitivity level 1							
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345
THB [(2)]	Temperature humidity bias							
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80
TC [(2)]	Temperature cycling							
	AEC-Q100-JESD22-A104	−65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80
TMSK [(2)]	Thermal shocks							
	JESD22-A106	−55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25
AC [(2)]	Autoclave (pressure pot)							
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80
HTSL [(2)]	High temperature storage life							
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
ELFR	Early life failure rate							
	AEC-Q100-008	HTOL 150 °C, 6 V	800	3	48 hrs	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)							
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-

1. See *Table 8: List of terms* for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 8. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
08-Sep-2010	1	First release.

Document Revision History		
Date	Rev.	Description of the Revision
September 06, 2010	1.00	First draft creation

Source Documents & Reference Documents		
Source document Title	**Rev.:**	**Date:**

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