# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM/10/5864
Notification Date 09/03/2010

**Capacity extension in the ST site of Longgang - China**
**for the DPAK, IPAK and PPAK packages**

**Table 1. Change Implementation Schedule**

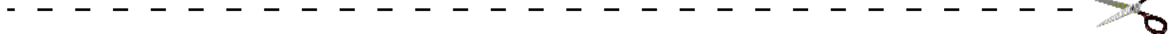
| | |
|---|---|
| Forecasted implementation date for change | 17-Oct-2010 |
| Forecasted availabillity date of samples for customer | 01-Oct-2010 |
| Forecasted date for **STMicroelectronics** change Qualification Plan results availability | 27-Aug-2010 |
| Estimated date of changed product first shipment | 03-Dec-2010 |

**Table 2. Change Identification**

| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | see attached list |
| Type of change | Package assembly location change |
| Reason for change | to increase our manufacturing capacity |
| Description of the change | In our progress to rationalize the manufacturing processes and progressively expand the production capacity, please be informed that products housed in the DPAK/IPAK/PPAK packages, currently manufactured in the Shenzhen (China) plant, will shortly be available from the site of Longgang (China). |
| Product Line(s) and/or Part Number(s) | See attached |
| Description of the Qualification Plan | See attached |
| Change Product Identification | see annex |
| Manufacturing Location(s) | |

**Table 3. List of Attachments**

| | |
|---|---|
| Customer Part numbers list | |
| Qualification Plan results | |



| Customer Acknowledgement of Receipt | PCN APM/10/5864 |
|---|---|
| Please sign and return to STMicroelectronics Sales Office | Notification Date 09/03/2010 |
| ☐ Qualification Plan Denied | Name: |
| ☐ Qualification Plan Approved | Title: |
| | Company: |
| ☐ Change Denied | Date: |
| ☐ Change Approved | Signature: |

Remark

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# DOCUMENT APPROVAL

| Name | Function |
|---|---|
| Giuffrida, Antonino | Division Marketing Manager |
| Caizzone, Francesco | Division Product Manager |
| Vitali, Gian Luigi | Division Q.A. Manager |

**WHAT**:

In our progress to rationalize the manufacturing processes and progressively expand the production capacity, please be informed that products housed in the DPAK/IPAK/PPAK packages, currently manufactured in the Shenzhen (China) plant, will shortly be available from the site of Longgang (China).

For the complete list of the part numbers affected by this change, please refer to the attached Products list.

**WHY:**

To increase our manufacturing global capacity for a better service to our customers on the affected products, by optimizing ST's leading-edge Longgang packaging and testing facility in China.

**HOW:**

This capacity expansion will be achieved by keeping **same processes** and **B.O.M** (Bill of materials) currently used in the Shenzhen Site, maintaining unaltered the **electrical**, **dimensional** and **thermal** parameters and keeping all information reported in the relevant product-datasheets, unchanged.
There is as well no variations in the **packing process** and in the **standard delivery quantities** either. All verifications are included in the qualification programs.

The preconditioning tests before reliability testing for the **DPAK/PPAK** packages have been performed following the **J-STD-020-D** recommendation for **MSL 1**.

The products will be delivered from the Longgang Site, will be compliant with the RoHS* directive (ECOPACK®1 ST grade).

*(*) Restriction of the use of certain Hazardous Substances*

**Qualification program and results**:

The qualification program consists of comparative **electrical characterizations** and **reliability tests**. The **preliminary reliability reports** for the transferred assembly line are annexed to the present document.

**WHEN:**

The final reliability reports will be available on request from October 1st 2010, therefore, Then massive production from the Longgang Site, is planned for the end of Q4-2010.

**Samples of test vehicles** are available now**. Other samples** of devices produced in the Longgang plant will be available on request from **October 1st 2010**.

Production start and first shipments will occur as indicated in the table below.

| Product sub-Family | 1st Shipments |
|---|---|
| **All involved devices** | From **Week 48-2010** |

Following Jedec Standard No. 46-C, lack of acknowledgement of the PCN within **30 days** will constitute acceptance of the change. After acknowledgement, lack of additional response within the **90 day period** from PCN notification will constitute acceptance of the change. In any case, first shipments may start earlier with customer's **written agreement**.

**MARKING AND TRACEABILITY:**

Unless otherwise stated by customer specific requirement, parts assembled in the Longgang plant will be indicated as below:

| Assembly location | Assy plant | Seq. nbr | Diffusion plant | Country of origin | Date Code (3 digits) |
|---|---|---|---|---|---|
| **Longgang (New)** | **G4** | LLL | XX | CHN | YWW<br>Y = 1 digit indicating the year<br>WW = 2 digits indicating the week number |

The full traceability of the parts assembled in the Longgang plant will be ensured by the **date code** by an **internal codification**, and by the **Q.A. number**.

Annex: Preliminary Reliability Reports

# Reliability Evaluation Report on

## *DPAK Package assembled in LGG*

## *EME-7026 Molding compound*

## *T.V.: LD1117DTTR, KSAD line*

| General Information | |
|---|---|
| **Product Line** | KSAD |
| **Product Description** | RGGR*KSADAA6 |
| **P/N** | LD1117DTTR |
| **Product Group** | APM |
| **Product division** | IPC VR |
| **Package** | DPAK |
| **Silicon Process technology** | BIP |

| Locations | |
|---|---|
| **Wafer fab** | *AMK6* |
| **Assembly plant** | *LGG* |
| **Reliability Lab** | *Catania* |
| **Reliability assessment** | *Pass* |

## DOCUMENT INFORMATION

| Version | Date | Pages | Prepared by | Approved by | Comment |
|---|---|---|---|---|---|
| 1.0 | 20-August-2010 | 8 | Alfio Rao | Giovanni Presti | Preliminary Report |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| **JESD47** | Stress-Test-Driven Qualification of Integrated Circuits |
| **AEC-Q100** | Stress test qualification for automotive grade integrated circuits |

# 2 GLOSSARY

| | |
|---|---|
| **DUT** | Device Under Test |
| | |
| **SS** | Sample Size |

# 3 RELIABILITY EVALUATION OVERVIEW

## 3.1 Objectives

To qualify DPAK line in LGG assembly plant.
Test Vehicle: *KSAD - LD1117DTTR, Std* resin EME-7026

## 3.2 Conclusion

Preliminary reliability results are positive

# 4 DEVICE CHARACTERISTICS

## 4.1 Device description

The LD1117 is a low drop voltage regulator able to provide up to 800 mA of output current, available even in adjustable version (VREF = 1.25 V). Concerning fixed versions, are offered the following output voltages: 1.2 V, 1.8 V, 2.5 V, 2.85 V, 3.0 V, 3.3 V and 5.0 V. The 2.85 V type is ideal for SCSI-2 lines active termination.

## 4.2 Construction note

| | P/N: LD1117DTTR |
|---|---|
| **Wafer/Die fab. information** | |
| Wafer fab manufacturing location | AMK6 6" |
| Technology | BIPOLAR |
| Process family | BIPOLAR |
| Die finishing back side | CHROMIUM/NICKEL/GOLD |
| Die size | 1990,1860 um |
| Bond pad metallization layers | 1 |
| Passivation type | SiN |
| | |
| **Wafer Testing (EWS) information** | |
| Electrical testing manufacturing location | APEE Asia Pac EWS |
| Tester | QT200 |
| Test program | KSXXEQXX.CTS vers. WAD |
| **Assembly information** | |
| Assembly site | LGG |
| Package description | TO-252 DPAK Cu Wire |
| Molding compound | SUMITOMO EME7026 |
| Die attach process | SOLF SOLDER |
| Die attach material | Pb/Ag/Sn 95.5/2.5/2 D.76mm SSD(5XP92057) |
| Die pad size | 3.0 x 4.2mm |
| Wire bonding process | Thermosonic Bonding Copper wire |
| Wires bonding materials/diameters | 1.5MIL Cu wire |
| Lead finishing/bump solder material | 100% Sn plating |
| **Final testing information** | |
| Testing location | STS |
| Tester | QT200 |
| Test program | KSX2FAAD.CTS |

# 5 TESTS RESULTS SUMMARY

## 5.1 Test vehicle

**P/N: LD1117DTTR**

| Lot | Diffusion Lot | Assy Lot | Trace Code | Process/ Package | Product Line | Comments |
|---|---|---|---|---|---|---|
| 1 | V6007EE7 | KSAD01N | RGGR*KSADAA6 | DPAK | KSAD | |
| 2 | V6007EE7 | KSAD02N | RGGR*KSADAA6 | DPAK | KSAD | |
| 3 | V6004KLJ | KSAD03N | RGGR*KSADAA6 | DPAK | KSAD | |

## 5.2 Test plan and results summary

**P/N: LD1117DTTR**

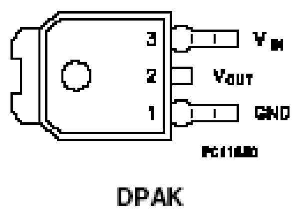
| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Lot 1 | Lot 2 | Lot 3 | |
| **Die Oriented Tests** | | | | | | | | | |
| HTB | N | JESD22 A-108 | Tj = 125°C, BIAS= +15 V | | 168 H | 0/77 | - | - | |
| | | | | | 500 H | 0/77 | - | - | |
| | | | | | 1000 H | running | - | - | |
| HTSL | N | JESD22 A-103 | Ta = 150°C | | 168 H | 0/45 | 0/45 | 0/45 | |
| | | | | | 500 H | 0/45 | 0/45 | 0/45 | |
| | | | | | 1000 H | running | running | running | |
| **Package Oriented Tests** | | | | | | | | | |
| PC | | JESD22 A-113 | Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3times | | Final | Pass | | | |
| | | | | | Final | | Pass | | |
| | | | | | Final | | | Pass | |
| AC | Y | JESD22 A-102 | Pa=2Atm / Ta=121°C | | 96h | 0/77 | 0/77 | 0/77 | |
| TC | Y | JESD22 A-104 | Ta = -65°C to 150°C | | 100 cy | 0/77 | 0/77 | 0/77 | |
| | | | | | 200 cy | 0/77 | 0/77 | 0/77 | |
| | | | | | 500 cy | running | running | running | |
| THB | Y | JESD22 A-101 | Ta = 85°C, RH = 85%, BIAS= +12 V | | 168 H | 0/77 | 0/77 | 0/77 | |
| | | | | | 500 H | 0/77 | 0/77 | 0/77 | |
| | | | | | 1000 H | running | running | running | |

# 6 ANNEXES

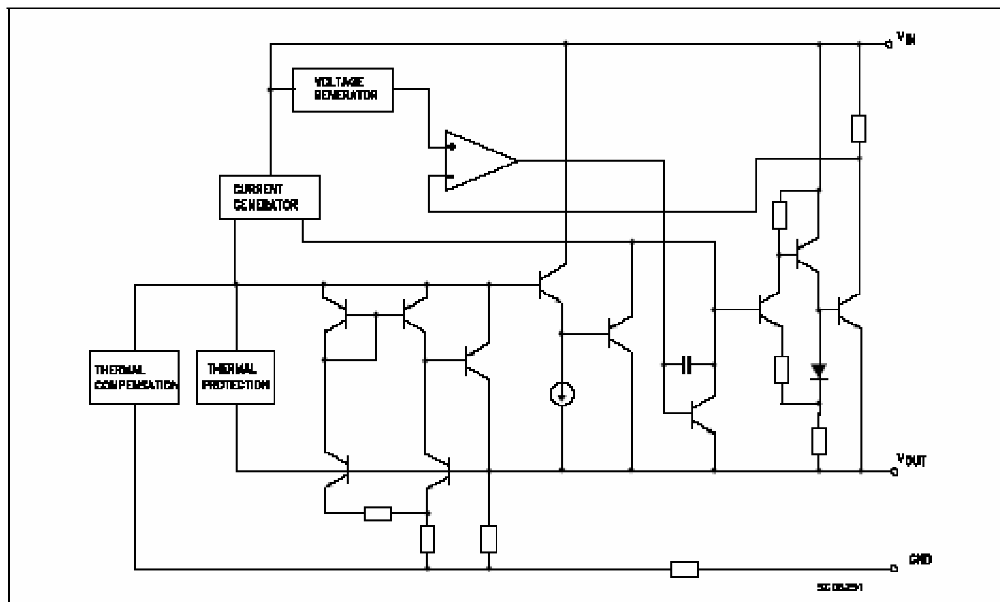
## 6.1 Device details

### 6.1.1 Pin connection

**Pin connections (top view)**

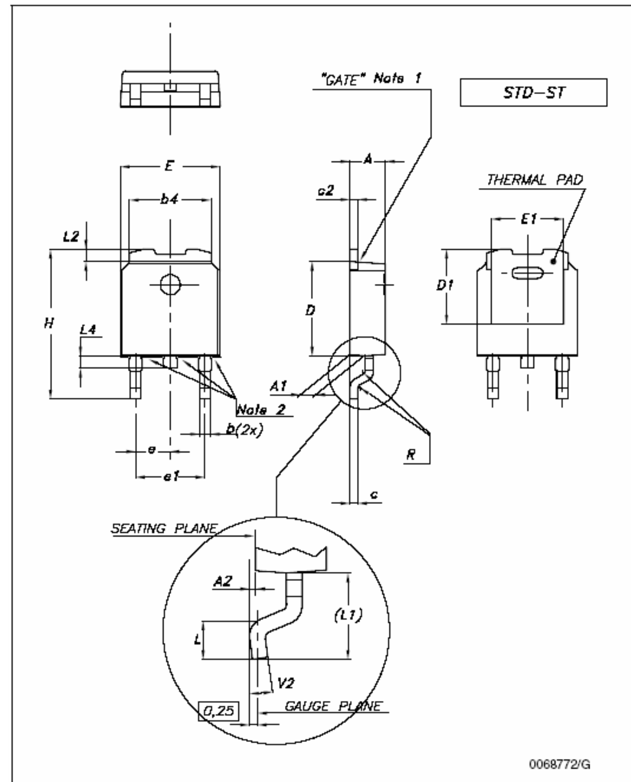



### 6.1.2 Block diagram



### 6.1.3 Package outline/Mechanical data

| Dim. | Type STD-ST | | |
|---|---|---|---|
| | mm. | | |
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | | 5.10 | |
| E | 6.40 | | 6.60 |
| E1 | | 4.70 | |
| e | | 2.28 | |
| e1 | 4.40 | | 4.60 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | |
| L1 | | 2.80 | |
| L2 | | 0.80 | |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |




Note: 1 Maximum resin gate protrusion: 0.5 mm.
2 Maximum resin protrusion: 0.25 mm.

## 6.2 Tests Description

| Test name | Description | Purpose |
|---|---|---|
| **Die Oriented** | | |
| **HTB**<br>High Temperature Bias | The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition. | To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.<br>The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults. |
| **HTSL**<br>High Temperature Storage Life | The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature. | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding. |
| **Package Oriented** | | |
| **PC**<br>Preconditioning | The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption. | As stand-alone test: to investigate the moisture sensitivity level.<br>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.<br>The typical failure modes are "pop corn" effect and delamination. |
| **AC**<br>Auto Clave (Pressure Pot) | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |
| **TC**<br>Temperature Cycling | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation. |
| **THB**<br>Temperature Humidity Bias | The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity. | To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence. |

# Reliability Evaluation Report

## *QUALIFICATION DPAK / IPAK LGG*

| General Information | |
|---|---|
| **Product Line** | *PL 58* |
| **Product Description** | *SCR, Triac & ACS* |
| **P/N** | *All AC Switches in DPAK/ IPAK packages* |
| **Product Group** | *IMS* |
| **Product division** | *APM* |
| **Package** | *DPAK* |
| **Silicon Process technology** | *Planar, mesa and top glass* |

| Locations | |
|---|---|
| **Wafer fab** | *ST TOURS (France)* |
| **Assembly plant** | *ST LONGGANG (china)* |
| **Reliability Lab** | *ST TOURS (France)* |
| **Reliability assessment** | *Pass* |

## DOCUMENT INFORMATION

| Version | Date | Pages | Prepared by | Approved by | Comment |
|---|---|---|---|---|---|
| 1 | 08/19/10 | 8 | Samuel Ducret | Guy Cazaubon | First issue |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| **JESD47** | Stress-Test-Driven Qualification of Integrated Circuits |

# 2 GLOSSARY

| | |
|---|---|
| **DUT** | Device Under Test |
| **PCB** | Printed Circuit Board |
| **SS** | Sample Size |
| **PC** | Pre-conditionning |
| **TC** | Temperature Cycling |
| **PCT** | Pressure Pot 2 bars |
| **PC** | Preconditionning |

# 3 RELIABILITY EVALUATION OVERVIEW

## 3.1 Objectives

The objective of this project is to qualify the DPAK/IPAK in LGG for the Scr's, the Triacs and the ACS parts. The assembly process of these parts will be transferred from STS standard DPAK line to LGG.

This reliability plan includes T835-600B/B, ACS120-7SB/B and TN1515-600BTR/B parts.

## 3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure).
Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.
So these preliminary reliability results are positive.

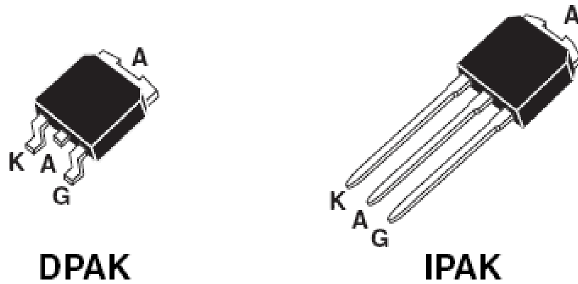
# 4 DEVICE CHARACTERISTICS

## 4.1 Device description

The Vehicules tests are the:

- T835-600B/B from the triac family with a DPAK package.
- ACS120-7SB/B from the ACS family with a DPAK package.
- TN1515-600BTR/B from the SCR family with a DPAK package.

See referenced Datasheet document from more information.




## 4.2 Construction note

See referenced Product Baseline for detailed information.

| | T835-600B-TR/7K |
|---|---|
| **Wafer/Die fab. information** | |
| Wafer fab manufacturing location | *ST TOURS (France)* |
| Technology | Mesa |
| Process family | Triacs |
| **Wafer Testing (EWS) information** | |
| Electrical testing manufacturing location | *ST TOURS (France)* |
| **Assembly information** | |
| Assembly site | *ST LONGGANG (china)* |
| Package description | DPAK |
| Molding compound | Epoxy resin |
| **Final testing information** | |
| Testing location | ST SHENZHEN (China) |

| | **TN1515-600BTR/7K** |
|---|---|
| **Wafer/Die fab. information** | |
| Wafer fab manufacturing location | *ST TOURS (France)* |
| Technology | Top glass |
| Process family | SCR |
| **Wafer Testing (EWS) information** | |
| Electrical testing manufacturing location | *ST TOURS (France)* |
| **Assembly information** | |
| Assembly site | *ST LONGGANG (china)* |
| Package description | DPAK |
| Molding compound | Epoxy resin |
| **Final testing information** | |
| Testing location | ST SHENZHEN (China) |

| | **ACS120-7SB-TR/7** |
|---|---|
| **Wafer/Die fab. information** | |
| Wafer fab manufacturing location | *ST TOURS (France)* |
| Technology | Planar |
| Process family | ACS |
| **Wafer Testing (EWS) information** | |
| Electrical testing manufacturing location | *ST TOURS (France)* |
| **Assembly information** | |
| Assembly site | *ST LONGGANG (china)* |
| Package description | DPAK |
| Molding compound | Epoxy resin |
| **Final testing information** | |
| Testing location | ST SHENZHEN (China) |

# 5 TESTS RESULTS SUMMARY

## 5.1 Test vehicle

| Lot # | Diffusion Lot | Process/ Package | Part number | Comments |
|---|---|---|---|---|
| 1 | VU952M44 | DPAK | T835-600B-TR/7K | Qualification lot |
| 2 | VU926M13 | DPAK | TN1515-600BTR/7K | Qualification lot |
| 3 | VU010096 | DPAK | ACS120-7SB-TR/7 | Qualification lot |

Detailed results in below chapter will refer to P/N and Lot #.

## 5.2 Test plan and results summary

**T835-600B-TR/7K**

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS Lot 1 | Note |
|---|---|---|---|---|---|---|---|
| package Oriented Tests | | | | | | | |
| Precond | Y | JESD22 A-113 | Eval MSL1:<br>Store 168 H @ Ta=85°C Rh=85%<br>Over Reflow @ Tpeak=260°C 3times | 25 | Final test at 25DC | 0/25 | MSL1 compliant |
| TC | Y | JESD22 A-104 | Ta= [-65C +150C]; 2cycles/hours | 25 | 100 cycles | 0/25 | |
| | | | | | 350 cycles | 0/25 | |
| U-HAST | Y | JESD22-A110-B | 130C 85%HR 2,3 BAR | 25 | 96h | 0/25 | |

**TN1515-600BTR/7K**

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS Lot 2 | Note |
|---|---|---|---|---|---|---|---|
| package Oriented Tests | | | | | | | |
| Precond | Y | JESD22 A-113 | Eval MSL1:<br>Store 168 H @ Ta=85°C Rh=85%<br>Over Reflow @ Tpeak=260°C 3times | 25 | Final test at 25DC | 0/25 | MSL1 compliant |
| TC | Y | JESD22 A-104 | Ta= [-65C +150C]; 2cycles/hours | 25 | 100 cycles | 0/25 | |
| | | | | | 350 cycles | 0/25 | |
| U-HAST | Y | JESD22-A110-B | 130C 85%HR 2,3 BAR | 25 | 96h | 0/25 | |

**ACS120-7SB-TR/7**

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS Lot 3 | Note |
|---|---|---|---|---|---|---|---|
| package Oriented Tests | | | | | | | |
| Precond | Y | JESD22 A-113 | Eval MSL1:<br>Store 168 H @ Ta=85°C Rh=85%<br>Over Reflow @ Tpeak=260°C 3times | 25 | Final test at 25DC | 0/25 | MSL1 compliant |
| TC | Y | JESD22 A- | Ta= [-65C +150C]; 2cycles/hours | 25 | 100 cycles | 0/25 | |

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | Note |
|---|---|---|---|---|---|---|---|
| | | | | | | Lot 3 | |
| | | 104 | | | 350 cycles | 0/25 | |
| U-HAST | Y | JESD22-A110-B | 130C 85%HR 2,3 BAR | 25 | 96h | 0/25 | |

Note : All the preconditioning have been done with the MSL1 condition

# 6 ANNEXES

## 6.1 Tests Description

| Test name | Description | Purpose |
|---|---|---|
| **Die Oriented** | | |
| **Package Oriented** | | |
| **PC**<br>Preconditioning | The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption. | As stand-alone test: to investigate the moisture sensitivity level.<br>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.<br>The typical failure modes are "pop corn" effect and delamination. |
| **U-HAST** | The device is not biased under 130°C 85% RH during 96 hours, or equivalent 110°C 85% RH during 264 hours, minimizing its internal power dissipation. | The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the "85/85" Steady-State Humidity Life Test (THB). |
| **TC**<br>Temperature Cycling | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation. |

# Reliability Report On Assembly and Testing Location Transfer within China from Shenzhen to Long Gang for DPAK package

| General Information | |
|---|---|
| **Product Lines** | BA19-EL6C-EZ62-EZ82 |
| **Product Description** | N-Channel Power MOSFET<br>NPN Power BIPOLAR |
| **Commercial Products** | MJD3055T4<br>STD20NF06LT4<br>STD4NK60ZT4<br>STD3NK80ZT4 |
| **Product Group** | IMS – APM |
| **Product division** | Power Transistor Division |
| **Package** | DPAK |
| **Silicon Process technology** | N-Channel Power MOSFET<br>NPN Power BIPOLAR |

| Locations | |
|---|---|
| **Wafer fab** | *BA19 / EZ82*<br>*Ang Mo Kio (Singapore)*<br><br>*EL6C / EZ62*<br>*Catania (ITALY)* |
| **Assembly plant** | *LONGGANG (China)* |
| **Reliability Lab** | *IMS-APM Catania Reliability Lab* |

## DOCUMENT INFORMATION

| Version | Date | Pages | Prepared by | Approved by | Comment |
|---|---|---|---|---|---|
| 1.0 | August-2010 | 12 | G.Montalto | G.Falcone | First issue |
| | | | | | |
| | | | | | |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| **JESD47** | Stress-Test-Driven Qualification of Integrated Circuits |
| | |

# 2 GLOSSARY

| | |
|---|---|
| **DUT** | Device Under Test |
| **SS** | Sample Size |
| | |

# 3 RELIABILITY EVALUATION OVERVIEW

## 3.1 Objectives

Qualifications of Long Gang as Assembly and Testing Location for DPAK package.

## 3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

# 4 DEVICE CHARACTERISTICS

## 4.1 Device description

Power Bipolar, Power MOSFET technology.

## 4.2 Construction note

**D.U.T.: MJD3055T4 LINE: BA19 PACKAGE: DPAK**

| **Wafer/Die fab. Information** | |
|---|---|
| Wafer fab manufacturing location | *AMK (Singapore)* |
| Technology | Planar NPN Power BIPOLAR |
| Die finishing back side | AuAs/Cr/Ni/Au |
| Die size | 2240 x 1940 um |
| Metal | Al/Si |
| Passivation type | P-Vapox |

| **Wafer Testing (EWS) information** | |
|---|---|
| Electrical testing manufacturing location | *AMK (Singapore)* |
| Test program | WPIS |

| **Assembly information** | |
|---|---|
| Assembly site | *LONGGANG (China)* |
| Package description | DPAK |
| Molding compound | Epoxy Resin |
| Frame material | Raw Copper - Frame coating Ni/NiP |
| Die attach process | Soft Solder |
| Die attach material | Pb/Sn/Ag |
| Wire bonding process | Ultrasonic |
| Wires bonding materials | 7 mils Al Base – 10 mils Al Emitter |
| Lead finishing/bump solder material | Pure Tin |

| **Final testing information** | |
|---|---|
| Testing location | *LONGGANG (China)* |
| Tester | IP TEST |

## D.U.T.: STD20NF06LT4 LINE: EL6C PACKAGE: DPAK

| Wafer/Die fab. Information | |
|---|---|
| Wafer fab manufacturing location | *Catania (ITALY)* |
| Technology | Power MOSFET STripFET Technology |
| Die finishing back side | Ti-Ni-Au |
| Die size | 2550x1950 um |
| Metal | Al/Si |
| Passivation type | None |

| Wafer Testing (EWS) information | |
|---|---|
| Electrical testing manufacturing location | *Catania (ITALY)* |
| Test program | WPIS |

| Assembly information | |
|---|---|
| Assembly site | *LONGGANG (China)* |
| Package description | DPAK |
| Molding compound | Epoxy Resin |
| Frame material | Raw Copper - Frame coating Ni/NiP |
| Die attach process | Soft Solder |
| Die attach material | Pb/Ag/Sn |
| Wire bonding process | Ultrasonic |
| Wires bonding materials | 5 mils Al/Mg Gate Pad – 10 mils Al Source Pad |
| Lead finishing/bump solder material | Pure Tin |

| Final testing information | |
|---|---|
| Testing location | *LONGGANG (China)* |
| Tester | IP TEST |

## D.U.T.: STD4NK60ZT4 LINE: EZ62 PACKAGE: DPAK

| Wafer/Die fab. information | |
|---|---|
| Wafer fab manufacturing location | *Catania (ITALY)* |
| Technology | Power MOSFET SuperMESH Technology |
| Die finishing back side | Ti-Ni-Au |
| Die size | 3180x2650 um |
| Metal | Al/Si |
| Passivation type | Nitride |

| Wafer Testing (EWS) information | |
|---|---|
| Electrical testing manufacturing location | *Catania (ITALY)* |
| Test program | WPIS |

| Assembly information | |
|---|---|
| Assembly site | *LONGGANG (China)* |
| Package description | DPAK |
| Molding compound | Epoxy Resin |
| Frame material | Raw Copper - Frame coating selected Ni |
| Die attach process | Soft Solder |
| Die attach material | Pb/Ag/Sn |
| Wire bonding process | Termosonic |
| Wires bonding materials | 2 mils Cu |
| Lead finishing/bump solder material | Pure Tin |

| Final testing information | |
|---|---|
| Testing location | *LONGGANG (China)* |
| Tester | IP TEST |

## D.U.T.: STD3NK80ZT4 LINE: EZ82 PACKAGE: DPAK

| Wafer/Die fab. information | |
|---|---|
| Wafer fab manufacturing location | *AMK (Singapore)* |
| Technology | Power MOSFET SuperMESH Technology |
| Die finishing back side | Ti-Ni-Au |
| Die size | 3280x2680 um |
| Metal | Al/Si |
| Passivation type | Nitride |

| Wafer Testing (EWS) information | |
|---|---|
| Electrical testing manufacturing location | *AMK (Singapore)* |
| Test program | WPIS |

| Assembly information | |
|---|---|
| Assembly site | *LONGGANG (China)* |
| Package description | *DPAK* |
| Molding compound | Epoxy Resin |
| Frame material | Raw Copper - Frame coating Ni/NiP |
| Die attach process | Soft Solder |
| Die attach material | Pb/Ag/Sn |
| Wire bonding process | Ultrasonic |
| Wires bonding materials | 5 mils Al/Mg - 10 mils Al Source Pad |
| Lead finishing/bump solder material | Pure Tin |

| Final testing information | |
|---|---|
| Testing location | *LONGGANG (China)* |
| Tester | IP TEST |

# 5 TESTS RESULTS SUMMARY

## 5.1 Test vehicle

| Lot # | Process/ Package | Product Line | Comments |
|---|---|---|---|
| 1 | MJD3055T4 | BA19 | Power BIPOLAR |
| 2 | STD20NF06LT4 | EL6C | Power MOSFET |
| 3 | STD4NK60ZT4 | EZ62 | Power MOSFET |
| 4 | STD3NK80ZT4 | EZ82 | Power MOSFET |

## 5.2 Reliability test plan and results summary

### D.U.T.: MJD3055T4 LINE: BA19 PACKAGE: DPAK

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Lot 1 | Lot 2 | Lot 3 | |
| **Die oriented test** | | | | | | | | | |
| **HTRB** | N | JEDD22 A-108 | T.A.=150℃, Bias 48V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **HTSL** | N | JESD22 A-103 | TA=150℃ | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **Package oriented tests** | | | | | | | | | |
| **PC** | - | JESD22-A113-B | DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% IR Reflow @ 260℃ 3 times | | Final | Pass | | | |
| **AC** | N | JESD22 A-102 | Pa=2Atm / Ta=121℃ | | 96 H | 0/77 | | | |
| **TC** | Y | JESD22 A-104 | TA=-65℃ TO +150℃ | 77 | 100 cy | 0/77 | | | |
| | | | | | 200 cy | 0/77 | | | |
| | | | | | 500 cy | Running | | | |
| **THB** | Y | JESD22 A-101 | TA=85℃, RH=85% Vbias=50V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |

## D.U.T.: STD20NF06LT4 LINE: EL6C PACKAGE: DPAK

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Lot 1 | Lot 2 | Lot 3 | |
| **Die oriented test** | | | | | | | | | |
| **HTRB** | N | JEDD22 A-108 | TA = 150°C, Vbias=48V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **HTFB** | N | JEDD22 A-108 | Tj=150°C, Vbias=20V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **HTSL** | N | JESD22 A-103 | TA=150°C | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **Package oriented tests** | | | | | | | | | |
| **PC** | - | JESD22-A113-B | DRYNG 24H @ 125°C<br>STORE 168H @ TA=85°C RH=85%<br>IR Reflow @ 260°C 3 times | | Final | Pass | | | |
| **AC** | N | JESD22 A-102 | Pa=2Atm / Ta=121°C | | 96 H | 0/77 | | | |
| **TC** | Y | JESD22 A-104 | TA=-65°C TO +150°C | 77 | 100 cy | 0/77 | | | |
| | | | | | 200 cy | 0/77 | | | |
| | | | | | 500 cy | Running | | | |
| **THB** | Y | JESD22 A-101 | TA=85°C, RH=85%<br>Vbias=50V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |

## D.U.T.: STD4NK60ZT4 LINE: EZ62 PACKAGE: DPAK

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Lot 1 | Lot 2 | Lot 3 | |
| **Die oriented test** | | | | | | | | | |
| **HTRB** | N | JEDD22 A-108 | TA = 150°C, Vbias=480V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **HTFB** | N | JEDD22 A-108 | Tj=150°C, Vbias=30V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **HTSL** | N | JESD22 A-103 | TA=150°C | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **Package oriented tests** | | | | | | | | | |
| **PC** | - | JESD22-A113-B | DRYNG 24H @ 125°C<br>STORE 168H @ TA=85°C RH=85%<br>IR Reflow @ 260°C 3 times | | Final | Pass | | | |
| **AC** | N | JESD22 A-102 | Pa=2Atm / Ta=121°C | | 96 H | 0/77 | | | |
| **TC** | Y | JESD22 A-104 | TA=-65°C TO +150°C | 77 | 100 cy | 0/77 | | | |
| | | | | | 200 cy | 0/77 | | | |
| | | | | | 500 cy | Running | | | |
| **THB** | Y | JESD22 A-101 | TA=85°C, RH=85%<br>Vbias=100V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |

## D.U.T.: STD3NK80ZT4 LINE: EZ82 PACKAGE: DPAK

| Test | PC | Std ref. | Conditions | SS | Steps | Failure/SS | | | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Lot 1 | Lot 2 | Lot 3 | |
| **Die oriented test** | | | | | | | | | |
| **HTSL** | N | JESD22 A-103 | TA=150℃ | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |
| **Package oriented tests** | | | | | | | | | |
| **PC** | - | JESD22-A113-B | DRYNG 24H @ 125℃<br>STORE 168H @ TA=85℃ RH=85%<br>IR Reflow @ 260℃ 3 times | | Final | Pass | | | |
| **AC** | N | JESD22 A-102 | Pa=2Atm / Ta=121℃ | | 96 H | 0/77 | | | |
| **TC** | Y | JESD22 A-104 | TA=-65℃ TO +150℃ | 77 | 100 cy | 0/77 | | | |
| | | | | | 200 cy | 0/77 | | | |
| | | | | | 500 cy | Running | | | |
| **THB** | Y | JESD22 A-101 | TA=85℃, RH=85%<br>Vbias=100V | 77 | 168 H | 0/77 | | | |
| | | | | | 500 H | 0/77 | | | |
| | | | | | 1000 H | Running | | | |

# ANNEXES 6.0

## 6.1Tests Description

| Test name | Description | Purpose |
|---|---|---|
| **HTRB**<br>High Temperature Reverse Bias<br><br>**HTGB**<br>High Temperature Forward (Gate) Bias | The device is stressed in static configuration, trying to satisfy as much as possible the following conditions:<br>• low power dissipation;<br>• max. supply voltage compatible with diffusion process and internal circuitry limitations; | To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.<br>To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. |
| **HTSL**<br>High Temperature Storage Life | The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature. | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding. |
| **AC**<br>Auto Clave<br>(Pressure Pot) | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |
| **TC**<br>Temperature Cycling | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation. |
| **THB**<br>Temperature Humidity Bias | The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity. | To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence. |

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