

# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-DIS/10/5788 Notification Date 08/06/2010

APM - ASD & IPAD Division CLT3-4BT6(-TR) quad digital termination 6" wafer conversion in Singapore plant

| Table 1. | Change | Implementation | Schedule |
|----------|--------|----------------|----------|
|----------|--------|----------------|----------|

| Forecasted implementation date for change   | 30-Jul-2010 |
|---|-------------|
| Forecasted availabillity date of samples for customer   | 30-Jul-2010 |
| Forecasted date for <b>STMicroelectronics</b><br>change Qualification Plan results availability | 30-Jul-2010 |
| Estimated date of changed product first shipment  | 01-Nov-2010 |

#### Table 2. Change Identification

| Product Identification<br>(Product Family/Commercial Product) | CLT3-4BT6(-TR) quad digital termination   |
|---|---|
| Type of change  | Product design change   |
| Reason for change   | increase production capacity  |
| Description of the change                                     | As a result of the constant investments made by STMicroelectronics in its technology evolution, the company is now implementing the 6 inch wafer size for the diffusion process in its Singapore plant for the CLT3-4BT6(-TR) device. With this 6 inch wafer expansion, STMicroelectronics increases its production capacity to better serve its customers through service improvement and lead time reduction, especially as volumes grow. |
| Product Line(s) and/or Part Number(s)                         | See attached  |
| Description of the Qualification Plan                         | See attached  |
| Change Product Identification                                 | date code, internal codification and QA number  |
| Manufacturing Location(s)                                     |   |

#### Table 3. List of Attachments

| Customer Part numbers list |  |
|----------------------------|--|
| Qualification Plan results |  |

| Customer Acknowledgement of Receipt                       | PCN APM-DIS/10/5788          |
|---|------------------------------|
| Please sign and return to STMicroelectronics Sales Office | Notification Date 08/06/2010 |
| Qualification Plan Denied                                 | Name:                        |
| Qualification Plan Approved                               | Title:                       |
|   | Company:                     |
| Change Denied   | Date:                        |
| Change Approved   | Signature:                   |
| Remark  |                              |
|   |                              |
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|   |                              |

| Name           | Function                   |
|----------------|----------------------------|
| Paris, Eric    | Division Marketing Manager |
| Duclos, Franck | Division Product Manager   |
| Cazaubon, Guy  | Division Q.A. Manager      |

### **DOCUMENT APPROVAL**



## PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-DIS/10/5788

# APM - ASD & IPAD Division<sup>1</sup>

# CLT3-4BT6(-TR) quad digital termination:

6 inch wafer conversion in Singapore plant



(1) APM: Analog, Power & MEMS Group - ASD: Application Specific Device - IPAD: Integrated Passive and Active Devices

#### WHY THIS CHANGE?

As a result of the constant investments made by STMicroelectronics in its technology evolution, the company is now implementing the **6 inch wafer size** for the diffusion process in its **Singapore plant** for the **CLT3-4BT6(-TR)** device.

With this 6 inch wafer expansion, STMicroelectronics increases its **production capacity** to better serve its customers through service improvement and lead time reduction, especially as volumes grow.

#### WHAT IS THE CHANGE?

This conversion to 6 inch wafers is achieved by migrating the current diffusion to the 6 inch process line already in place for several years. The conversion is using existing and qualified equipment in this plant.

This conversion has **no impact on the electrical parameters** of the products. The verification by characterization is included in the qualification program. **No other change** is affecting the manufacturing process.

There is **no change** in the **packing mode** and in the standard **delivery quantities**.

#### HOW AND WHEN?

#### Qualification program and results availability:

The qualification program mainly consists of comparative electrical characterizations and reliability tests.

The **qualification report** is annexed to this document.

#### Samples availability:

Samples are available on request from **now**.

#### Change implementation schedule:

The **production start** and **first shipments** will be implemented according to our work in progress and materials availability as indicated in the table below.

| <b>Production Start</b>  | 1st Shipments            |  |
|--------------------------|--------------------------|--|
| From Week <b>30-2009</b> | From Week <b>43-2010</b> |  |

Deliveries of **current product versions** will continue while the 6 inch conversion is brought to completion and as long as 5 inch stocks last.

Following Jedec Standard No. 46-C, lack of acknowledgement of the PCN within **30 days** will constitute acceptance of the change. After acknowledgement, lack of additional response within the **90 day** period from PCN notification will constitute acceptance of the change. In any case, **first shipments** may start earlier with customer's **written agreement**.

Marking and traceability:

The marking of the products remains unchanged.

The traceability for the modified products will be ensured by the date code, by an internal codification and by the Q.A. number.

R.

Annex: Related qualification reports

- **10132QRP**: Qualification of 6 inch Wafer Diameter in Singapore Plant



# Reliability Evaluation Report

CLT3-4BT6(-TR)/M1:

6" wafer conversion in Singapore plant

| General Information        |                 | Locations              |               |
|----------------------------|-----------------|------------------------|---------------|
| Product Description        | Control part    | Wafer fab              | ST AMK 6 inch |
| P/N                        | CLT3-4BT6-TR/M1 |                        |               |
| Product Group              | IMS             |                        |               |
| Product division           | APM             | Assembly plant         | Subcontractor |
| Package                    | TSSOP20         |                        |               |
| Silicon Process technology | BI20IIS         |                        |               |
| Maturity level step        | 30              | Reliability Lab        | ST            |
|                            |                 |                        |               |
|                            |                 | Reliability assessment | Pass          |
|                            |                 |                        |               |

### **DOCUMENT INFORMATION**

| Version | Date     | Pages | Prepared by | Approved by | Comment     |
|---------|----------|-------|-------------|-------------|-------------|
| 1       | 07/27/10 | 7     | S. Ducret   | G. Cazaubon | First issue |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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### **<u>1</u>** APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description                                       |
|--------------------|---|
| JESD47             | Stress-Test-Driven Qualification of Integrated Circuits |

### 2 GLOSSARY

| DUT  | Device Under Test                        |
|------|--|
| PCB  | Printed Circuit Board                    |
| SS   | Sample Size                              |
| PC   | Pre-conditionning                        |
| HTRB | High Temperature Reverse Bias            |
| тс   | Temperature Cycling                      |
| PCT  | Pressure Pot 2 bars                      |
| ТНВ  | Temperature Humidity Bias                |
| OLT  | Operational Life Test or Functional Test |



### **<u>3 RELIABILITY EVALUATION OVERVIEW</u>**

### 3.1 **Objectives**

The objective of this report is to evaluate the reliability impact of the conversion from 5 inch wafer size to 6 inch wafer size in Singapore plant for the CLT3-4BT6(-TR) device.

This conversion to 6 inch wafers is achieved by migrating the current CLT3-4BT6 diffusion to the 6 inch process line already in place and qualified for several years. The conversion is done using existing and qualified equipment in this plant. An electrical characterization has been done and shows that this conversion has no impact on the electrical parameters.

No other change is affecting the manufacturing process.

The current report leans on 6 inch BI20IIS similarities and uses generic data as evidence of reliability guarantee.

### 3.2 **Conclusion**

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



# 4 DEVICE CHARACTERISTICS

# 4.1 **Device description**

See referenced Datasheet document.

### 4.2 Construction note

See referenced Product Baseline for detailed information.

| _                                | CLT3-4BT6-TR/M |  |  |  |
|----------------------------------|----------------|--|--|--|
| Wafer/Die fab. information       |                |  |  |  |
| Wafer fab manufacturing location | STM AMK 6 inch |  |  |  |
| Technology                       | BI20IIS        |  |  |  |
| Assembly information             |                |  |  |  |
| Assembly site                    | Subcontractor  |  |  |  |
| Package description              | TSSOP20        |  |  |  |
| Molding compound                 | Epoxy resin    |  |  |  |
| Final testing information        |                |  |  |  |
| Testing location                 | Subcontractor  |  |  |  |
|                                  |                |  |  |  |



# 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicle

| Lot # | Finished<br>Good | Techno  | Comments                            |
|-------|------------------|---------|-------------------------------------|
| 1     | PCLT-2AT4        | BI20IIS | Similar F.E. technology<br>and B.E. |
| 2     | STCC02-BD5       | BI20IIS | Similar F.E. technology             |
| 3     | STCC05-BD4       | BI20IIS | Similar F.E. technology             |
| 4     | STCC08           | BI20IIS | Similar F.E. technology             |

Detailed results in below chapter will refer to P/N and Lot #.

### 5.2 Test plan and results summary

| Test               | PC          | Std ref                        | Std ref. Conditions SS   | SS         | Steps  | Failure/SS |       |       |       |
|--------------------|-------------|--------------------------------|--|------------|--------|------------|-------|-------|-------|
| 1031               |             | old fel.                       |  | 00         |        | Lot 1      | Lot 2 | Lot 3 | Lot 4 |
| package O          | riente      | d Tests                        |  |            |        |            |       |       |       |
| THB N              |             |                                |  |            | 168 H  | 0/152      | 0/40  | 0/40  | 0/231 |
|                    | JESD22A-101 | Ta = 85°C, RH = 85%, Bias      | 463  | 500 H      | 0/152  | 0/40       | 0/40  | 0/231 |       |
|                    |             |                                |  | 1000 H     | 0/152  | 0/40       | 0/40  | 0/231 |       |
| РСТ                | Y           | JESD22A-102                    | Temperature 121 °C<br>Pressure 2 bar<br>100% relative humidity | 198        | 96H    | 0/77       | 0/77  | 0/77  | 0/44  |
| TC Y JESD22A-104   |             | -65°C/+150°C;<br>2Cycles/hours | 539  | 100 cycles | 0/154  | 0/77       | 0/77  | 0/231 |       |
|                    | JESD22A-104 |                                |  | 500 cycles | 0/154  | 0/77       | 0/77  | 0/231 |       |
|                    |             |                                | 1000cycles   | 0/154      | 0/77   | 0/77       | 0/231 |       |       |
| Die Oriented Tests |             |                                |  |            |        |            |       |       |       |
| OLT N              |             | JESD22A-108                    | Bias, Tj max   | 240        | 168 H  | 0/30       | 0/60  | 0/120 | 0/30  |
|                    | Ν           |                                |  |            | 500 H  | 0/30       | 0/60  | 0/120 | 0/30  |
|                    |             |                                |  |            | 1000 H | 0/30       | 0/60  | 0/120 | 0/30  |



# 5.3 Test description

| Test name                           | Description  | Purpose  |  |  |
|-------------------------------------|--|--|--|--|
| Die Oriented                        |  |  |  |  |
| <b>OLT</b><br>Operating Life Test   | The device is stressed in dynamic<br>configuration, trying to satisfy as much as<br>possible the following conditions:<br>o Application stress condition.<br>o Max. operative supply voltage and worst<br>case operative voltage.<br>o Max. current load<br>o Max. operative junction temperature.<br>The typical failure modes are related to<br>electromigration, wire-bonds degradation,<br>oxide faults. | The objective of this test is to simulate the life<br>time of the device in the application and to verify<br>the compatibility of the die with the application<br>requirements   |  |  |
| Package Oriented                    |  |  |  |  |
| <b>PC</b><br>Preconditioning        | The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.  | As stand-alone test: to investigate the moisture<br>sensitivity level.<br>As preconditioning before other reliability tests:<br>to verify that the surface mounting stress does<br>not impact on the subsequent reliability<br>performance.<br>The typical failure modes are "pop corn" effect<br>and delamination.  |  |  |
| <b>TC</b><br>Temperature<br>Cycling | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.  | To investigate failure modes related to the<br>thermo-mechanical stress induced by the<br>different thermal expansion of the materials<br>interacting in the die-package system. Typical<br>failure modes are linked to metal displacement,<br>dielectric cracking, molding compound<br>delamination, wire-bonds failure, die-attach<br>layer degradation. |  |  |
| THB<br>Temperature<br>Humidity Bias | The device is biased in static configuration<br>minimizing its internal power dissipation,<br>and stored at controlled conditions of<br>ambient temperature and relative humidity.<br>85°C / RH=85% ; 1000 hours   | To evaluate the package moisture resistance<br>with electrical field applied, both electrolytic<br>and galvanic corrosion are put in evidence.   |  |  |
| PCT<br>Pressure<br>CookerTest       | Conditions: - Ta=121°C Pressure=2 atm;<br>100% RH for 96 hrs   | To point out critical water entry paths with consequent electrochemical and galvanic corrosion.  |  |  |

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