

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM/10/5472 Notification Date 03/25/2010

Capacity Expansion for DIP-8 package by using Copper wires process in the Shenzhen plant including ECOPAK2 Capability

Table 1. Change Implementation Schedule

Forecasted implementation date for change	07-Jun-2010
Forecasted availabillity date of samples for customer	22-Mar-2010
Forecasted date for STMicroelectronics change Qualification Plan results availability	18-Mar-2010
Estimated date of changed product first shipment	01-Jul-2010

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly process change
Reason for change	To increase productivity, improve service to Customers
Description of the change	Progressing in the plan for rationalizing the manufacturing processes and capacity expansion, Please be informed that the production lines for all products housed in the DIP-8 packages, cur-rently located in Shenzhen China plant, will be expanded by implementing, in addition to the in-use, Gold Wire, the already well consolidated Copper Wire process. The capacity expansion in the Shenzhen plant, will imply the supply of Ecopack2 products (also called Halogen Free). This process, Copper Wire and Ecopack2, will be progressively implemented for all the other similar packages and technologies in the ST's manufacturing sites, providing you timely in-formation via the relevant PCNs.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	See attached document
Manufacturing Location(s)	

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Table 3. L	ist of	Attachme	nts
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Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	PCN APM/10/5472
Please sign and return to STMicroelectronics Sales Office	Notification Date 03/25/2010
□ Qualification Plan Denied	Name:
□ Qualification Plan Approved	Title:
	Company:
□ Change Denied	Date:
□ Change Approved	Signature:
Remark	
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DOCUMENT APPROVAL

Name	Function
Lombardo, Mario	Division Marketing Manager
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Vitali, Gian Luigi	Division Q.A. Manager

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WHAT:

Dear ST Customer,

Progressing in the plan for rationalizing the manufacturing processes and capacity expansion, Please be informed that the production lines for all products housed in the DIP-8 packages, currently located in Shenzhen China plant, will be expanded by implementing, in addition to the in-use, Gold Wire, the already well consolidated Copper Wire process.

The capacity expansion in the Shenzhen plant, will imply the supply of Ecopack2 products (also called Halogen Free).

This process, Copper Wire and Ecopack2, will be progressively implemented for all the other similar packages and technologies in the ST's manufacturing sites, providing you timely information via the relevant PCNs.

The affected product series for this former step, are listed in the table below:

Product Family Code	Product Family	Product PN or Series
71	Standard Linears	LFxxx/LMxxx / MCxxx / TLxxx / TSxx / TSHxxx/UAxxx
32	Voltage Regulators	MC34063xxx
M9	Low Data rate Rf	ST485xxx

All STMicroelectronics devices housed in DIP-8 packages and manufactured in the Shenzhen plant, even though not expressly included in the above table, are affected by this change.

WHY:

To increase productivity, improve service to Customers and to optimize ST's assets utilization by enhancing the use of the leading-edge testing and packaging facility in Shenzhen - China. The Copper wire process will enhance also, operational efficiencies. (quality and cycle time improvement).

HOW:

By implementing the Copper wire process and expanding production in the ST's site of Shenzhen, China.

This capacity increase will not impact the electrical, thermal and dimensional parameters for ST's products, maintaining unchanged current information published in the relevant datasheets. There are as well no changes in the packing modes nor in the standard delivery quantities either.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

WHEN:

Production line transfer will be finalized within June_2010

Implementation schedule:

The samples, production start and first shipments will be implemented according to the following schedule:

Product Families	Samples	Production Start	1st Shipments
M9,32,71	Week 12'10(test vehicles) (*)	From Week 23-2010	From Week 26-2010

(*) Samples of any other samples out of the test vehicles, could be requested directly to the concerned Product Group.

Marking and traceability:

Unless otherwise stated by customer specific requirement, parts assembled using copper wire process, will maintain unchanged current marking.

The full traceability of the parts will be ensured by the date code, by an internal codification, and by the Q.A. number.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.

Please note that ST Team is doing all the best for providing a full visibility about the announced restructuring plan and to minimize any undesired consequences that may occur.

While our Marketing and Sales teams are available for any additional information, we are looking forward to your renewed confidence in STMicroelectronics as the strategic partner of your choice.

Sincerely Yours.







External Reliability Evaluation Report

Qualification type: Halogen free qualification

General Information		
Product Line	:	0082,393
Product Description	:	Dual op amp, Dual comparator
Commercial Product	:	TL082CN, LM393N
Product division/BU	:	APM/MSH/AMPS
Package : MiniDIP 8		
Technology process	:	Jfet, Bipolar

Locations		
Wafer fab location	Ang Mo Kio (singapore)	
EWS plant location	Toa Payoh (singapore)	
Assembly plant location:	ST Shenzhen (China)	
Final test plant location:	ST Shenzhen (China)	

DOCUMENT APPROVAL LIST

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DISTRIBUTION LIST

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DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
Α	10th March 2010	6	JM Bugnard	First release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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1 RELIABILITY and qualification evaluation overview

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on TL082CN and LM393N test vehicles to qualify new production line for AMPS (Analog, mixed product and services) produced in MiniDIP8 package in ST Shenzhen

1.2 Conclusion

All results are inside ST specification and the plan to achieve qualification exercise is described in below sections. The package MiniDIP8 halogen free including material described in below section, is qualified for AMPS business unit. For the qualification in order to have two sources for compound two molding compound Henkel and KCC have been evaluated. For both compound no reliability and mechanical issue was detected.

2 DEVICES TRACABILITY

2.1 <u>Devices description</u>

0082: The TL082, TL082A and TL082B are high speed JFET input dual operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

0393: This device consists of two independent low power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic: the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.

2.2 Wafer fabrication information

	TV1	TV2
Line	82	393
Wafer Fab location	Singapore	Singapore
FE process	Jfet	Bipolar
Die size (µm)	1570 x 1300	950 x 870
Die thickness (µm)	280	280
Metallization	AlSiCu	AlSiCu
Passivation	Si N + Pvapox	Si N
Back side	Raw Silicon	Raw Silicon

1.3 Assembly information

	Current process	Modified process
Assembly location	ST Shenzhen	ST Shenzhen
Die attach	ABLEBOND 8390 GLUE AEMBond FP-1725-0B	ABLEBOND 8390S-25
Wire	Gold 0.8 mils	Copper 1 mils
Leadframe	Copper 100x100mils Copper 110x140mils	Copper 100x100mils Copper 110x140mils
Molding compound	HYSOL MG46FAM SAMSUNG SI-7200DMA	KCC KTMC1000 1050GI Henkel GMC GR360A-ST
Lead finishing	Sn	Sn
Wafer thickness	280	280
Backgrinding location	Diffusion	Diffusion

Ref: QAMDCUK1



3 Reliability Tests results

3.1 <u>Test vehicle</u>

Lot#	Process/ Package	Product Line	Comments
1	Bipolar /MiniDIP8	393	with Henkel GMC GR360A-ST (SHZ lab)
2	Bipolar /MiniDIP8	393	with KCC KTMC1000 1050GI (SHZ lab)
3	Jfet /MiniDIP8	82	with Henkel GMC GR360A-ST (SHZ lab)
4	Jfet /MiniDIP8	82	with KCC KTMC1000 1050GI (SHZ lab)
5	Bipolar /MiniDIP8	393	with Henkel GMC GR360A-ST (GNB lab)
6	Bipolar /MiniDIP8	393	with KCC KTMC1000 1050GI (GNB lab)
7	Jfet /MiniDIP8	82	with Henkel GMC GR360A-ST (GNB lab)
8	Jfet /MiniDIP8	82	with KCC KTMC1000 1050GI (GNB lab)

Detailed results in below chapter will refer to P/N and Lot #.

3.2 Test plan and results summary

Shenzhen reliability laboratory

Tests	Conditions	Step	TV1	TV2	TV3	TV4	Comments
		Line	393	393	82	82	
Report reference			09CE581	09CE582	09CE585	09CE584	
	Lot reference		GK9441N6ZW	GK9441N6ZY	GK9441N7ZY	GK9441N7ZZ	
Die orientee	d tests						
	Tj=125℃		Ta=125	Ta=125	Ta=125	Ta=125	
HTB	Vs=absolute max rating	168h			0/78	0/78	Pass
	JESD22 A-108	1000h			0/78	0/78	Pass
Package or	iented tests						
	Ta=85C RH=85%	168h					
THB	Vs=nominal						
	JESD22 A-101	1000h					
AC	Ta=121C P=2atm	168h	0/78	0/78	0/78	0/78	Pass
AO	JESD22 A-102	240h	0/78	0/78	0/78	0/78	Pass
	Ta=-65/+150C JESD22 A-104	100cy	0/78	0/78	0/78	0/78	Pass
TMC		500cy	0/78	0/78	0/78	0/78	Pass
	0E0D22 / 104	1000cy	0/78	0/78	0/78	0/78	Pass





Grenoble reliability laboratory

Tests	Conditions	Step	TV5	TV6	TV7	TV8	Comments
		Line	393	393	82	82	
Report reference			09CE587	09CE580	09CE585	09CE584	
	Lot reference		GK9441N7ZV	GK9441N6ZZ	GK9441N7ZY	GK9441N7ZZ	
Die oriente	d tests						
	Tj=125℃		Ta=125	Ta=125	Ta=125	Ta=125	
HTB	Vs=absolute max rating	168h	0/78	0/78	0/78	0/78	Pass
	JESD22 A-108	1000h	0/78	0/78	0/78	0/78	Pass
Package or	riented tests						
THB	Ta=85C RH=85% Vs=nominal	168h	0/78	0/78	0/78	0/78	Pass
	JESD22 A-101	1000h	0/78	0/78	0/78	0/78	Pass
AC	Ta=121C P=2atm	168h	0/78	0/78	0/78	0/78	Pass
AC	JESD22 A-102	240h	0/78	0/78	0/78	0/78	Pass
	To- 65/1150C	100cy	0/78	0/78	0/78	0/78	Pass
TMC	Ta=-65/+150C JESD22 A-104	500cy	0/78	0/78	0/78	0/78	Pass
	0L0D22 // 104	1000cy	0/78	0/78	0/78	0/78	Pass
HTSL		168h	0/78	0/78	0/78	0/78	Pass
IIISL	Ta=150℃	1000h	0/78	0/78	0/78	0/78	Pass

4 Annexes

4.1 <u>Tests Description</u>

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
Package Oriented		
AC autoclave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Ref: QAMDCUK1



ESD Electro Static Discharge
ELFR Early Life Failure Rate

GL Gate Leakage

HTB High Temperature Bias

HTRB High Temperature Reverse BiasHTS High Temperature StorageT.H.B. Temperature Humidity Bias

T.C. Thermal CycleP.P. Pressure PotP.C. Preconditioning

Environmental sequence

Env. Seq.

WBS Wire Bond shear
WBP Wire bond Pull
SD Solderability

Ref: QAMDCUK1



5 Construction analysis

5.1 Ball Shear (5 units minimum 30 bonding AECQ100-001)

value in g

	TV1	TV2	TV3	TV4	TV5	TV6
Mean	39.3	38.1	41.6	40.2	41.0	40.9
Max	46.0	43.9	49.4	47.1	49.8	48.3
Min	33.4	31.1	31.1	33.6	35.1	33.2
Stddev	3.1	4.1	3.7	3.1	3.2	3.9
Cpk	2.5	1.8	2.2	2.6	2.6	2.1

5.2 Bond Pull (5 units minimum 30 bonding AECQ100-001)

value in g

	TV1	TV2	TV3	TV4	TV5	TV6
Mean	14.3	12.3	16.1	12.3	13.9	13.9
Max	16.3	15.6	18.9	14.3	15.7	15.7
Min	10.0	8.7	13.7	10.2	12.3	12.2
Stddev	1.5	1.3	1.3	1.2	0.9	1.0
Cpk	2.3	2.1	3.0	2.3	3.6	3.4

5.3 Solderability test

Spec Limit until area<5%

	TV1	TV2	TV3	TV4	TV5	TV6
SnPb bath with steam aging 8 Hrs	0/15	0/15	0/15	0/15	0/15	0/15
SnAgCu bath with steam aging 8 Hrs	0/15	0/15	0/15	0/15	0/15	0/15

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