PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-SLI/09/4948
Notification Date 09/24/2009

TS3022 Dual High Speed Comparator DESIGN CHANGE

Table 1. Change Implementation Schedule

Forecasted implementation date for change	17-Sep-2009
Forecasted availabillity date of samples for customer	17-Sep-2009
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	17-Sep-2009
Estimated date of changed product first shipment	24-Dec-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	TS3022 in all packages
Type of change	Product design change
Reason for change	Stability improvement
Description of the change	This current PCN is additional to PCN APM-SLI/08/4023 transfer CRN_UMC_HF5CMOS. This new PCN is related to a design change on TS3022 product: stability and vio improvement.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	In second part of trace code, letters "LE" as identification for UMC plant instead of VH for CRN6".
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	PCN APM-SLI/09/4948
Please sign and return to STMicroelectronics Sales Office	Notification Date 09/24/2009
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Gilot, Yves	Division Marketing Manager
Kaire, Jean-Claude	Division Product Manager
Paccard, Francoise	Division Q.A. Manager

Qualification Report

New product qualification

STMicroelectronics-APM Group -AMPS Business Unit

Product Line: **302201**

Description: **Dual rail to rail 1.8V high speed micropower comparator**

Product name: **TS3022**

DOCUMENT INFORMATION

Approval history

Revision 1

Activated on: Sep/11/2009 Issue after PCN ref.: APM-SLI/09/4948
Initiated by: CHASSAGNEUX Alain

Signator	Function	Approved on
CHASSAGNEUX Alain	Pdt Eng. manager	Sep/11/2009
JOURDAN Marie-Sophie	QA	Sep/11/2009

TABLE OF CONTENTS

1. Presentation & Main Results of Qualification

Presentation & main results of qualification

The TS3022 dual comparator features a high-speed response time with rail-to-rail inputs. With a supply voltage specified from 2V to 5V, this comparator can operate over a wide temperature range: -40°C to +125°C.

The TS3022 comparator offers micropower consumption as low as a few tens of microamperes thus providing an excellent ratio of power consumption current versus response time.

The TS3022 includes push-pull outputs and is available in small packages (SO-8 and MiniSO8).

Electrical results:

Product (lot)	Package/plant
TS3022IDT (LE848001) **TS3022IST** (LE848001)	SO8 / BOUSKOURA miniSO8 / CARSEM

The yield analysis conforms to ST standard results
Electrical parameters distribution on 50 pieces at T°AMB = 25°C and at cold and hot temperatures
The results conform to datasheet specifications.

ESD measurement:
The results conform to datasheet specifications (see ESD certificate).
The units have been tested at 25°C before and after electrostatic discharge.

Latch-up measurement was performed according to ST specification (n°0018695):
No latch-up was observed.
The units have been tested at 25°C before and after stress.

Design FMEA: *FMEA_3022.pdf*
Confidential document upon request with non-disclosure agreement (NDA).

Environmental and Quality information:
ST is certified ISO/TS16949:
certificate: 9136.STM2; approval authority IATF/CISQ-Auto.
ST Quality international awards:
EMAS & ISO 14001 OHSAS 18001 Environmental Management System; for all sites

Subcontractor certification:

	Automotive		Environmental	
Site	Certification	Number	Certification	Number
Carsem	TS16949	11764	ISO14001	C004101129

Quality and Reliability tests were performed according to the qualification plan

Reliability test	Nb of rejects	Package/plant	Test circuit
High Temperature Bias test (HTB) T° AMB = 125°C - Duration = 1000h TS3022IST (LE848001) TS3022IST (H605006) TS3022IDT (H605006) The units have been tested at 25°C before and after HTB	0/78 0/78 0/78	miniSO8/Carsem miniSO8/Carsem SO8/Bouskoura	N120NF N120NF N120NF
Temperature & Humidity bias (THB) Including preconditioning according to MSL 1 (J-STD-020 for SMD package). T°AMB = 85°C humidity = 85% Duration = 1000h TS3021ICT (H531420) TS922ID (1st lot) LM358IST (1st lot) The units have been tested at 25°C before and after THB	0/78 0/78 0/78	SC70-5/Carsem SO8/Bouskoura miniSO8/Carsem	N120NB N120GJ N120BA
Temperature cycling (TC) Including preconditioning according to MSL 1 (J-STD-020 for SMD package). T°AMB = -65/125°C Nb cycles = 1000 TS3021ICT (H531420) TS922ID (1st lot) LM358IST (1st lot) The units have been tested at 25°C before and after TC.	0/78 0/78 0/78	SC70-5/Carsem SO8/Bouskoura miniSO8/Carsem	Not applicable Not applicable Not applicable
Pressure pot test (PPT) Including preconditioning according to MSL 1 (J-STD-020 for SMD package). T°AMB = 121°C Pressure = 2atm - Duration = 240h TS3021ICT (H531420) TS922ID (1st lot) LM358IST (1st lot) The units have been tested at 25°C before and after PPT	0/78 0/78 0/78	SC70-5/Carsem SO8/Bouskoura miniSO8/Carsem	Not applicable Not applicable Not applicable

Conclusion

Electrical and reliability results meet or exceed the requirements set in the ST qualification program. The results conform to datasheet specifications and Product Qualification Plan PQP reference **ADCS_7685717.**
This device is qualified for the **SO8** and **miniSO8** packages.

Detailed results are available upon request
"WARNING": Tests results and information contained in this document are for information only. This document does not alter ST Microelectronics standard warranty or product specification.

2. Design Certification, Construction & Qualification

Q100 Certification of Design, Construction and Qualification

Supplier Name: ST Microelectronics
Supplier Part Number: TS3022IST

Item Name	Supplier Response
1. User's Part Number:	TS3022IST
2. Supplier's Part Number/Data Sheet:	TS3022IST / CD00222487
3. Die Fab Facility & Process ID:	UMC & HF5CMOS-AF30
4. Assembly Facility & Process ID:	CARSEM M & 7351968
5. Final Quality Control A (Test) Facility:	CARSEM S
6. Die:	
a. Die family:	N/A
b. Die mask set revision & name:	3022CA
7. Die Technology Description:	
a. Die channel length:	N/A
b. Die gate length:	N/A
c. Die process technology:	HF5CMOS
d. Die supplier process ID (Mask #):	HF5CMOS-AF30
e. Number of transistors or gates:	N/A
f. Number of mask steps:	23
8. Die Dimensions:	
a. Die width:	920 micron
b. Die length:	750 micron
c. Die thickness:	280 micron
9. Die Metallization:	
a. Die metallization material(s):	AlCu/TinArc - AlCu/TinArc - AlCu/TinArc
b. Number of layers:	3
c. Thickness (per layer):	0.55 micron / 0.55 micron / 0.85 micron
d. % of alloys (if present):	N/A
10. Die Passivation:	
a. Number of passivation layers:	See 10b.
b. Die passivation material(s):	PSG + NITRIDE
c. Thickness(es) & tolerances:	N/A
11. Pictorial Cross-Section:	See attached ☐ Not available ☒
12. Die Prep Backside:	
a. Die prep method:	See 12b.
b. Die metallization:	LAPPED SILICON
c. Thickness(es) & tolerances:	N/A
13. Die Separation Method (Kerf Depth):	100% Sawing
14. Die Attach:	
a. Die attach material ID:	Ablebond 84-1LMISR4
b. Die attach method:	Epoxy glue
15. Package:	
a. Type of package:	MSOP/TSSOP 8 BODY3.00 PITCH0.65
b. Ball/lead count:	See 15a.
16. Mold Compound:	
a. Mold compound supplier & ID:	Sumitomo 6600
b. Flammability rating:	UL 94 V1 ☐ UL 94 V0 ☒
c. Mold compound type:	Epoxy
d. MSL level (if known):	1

17. Wire Bond: a. Wire bond material: b. Wire bond diameter (mils):	 GOLD 1 MILS 1
18. Wire Bond Diagram:	Bonding diagram reference : 7757466 attached ☐
19. Wire Bond: a. Type of wire bond at die: b. Type of wire bond at leadframe:	 Ball Bonding Stitch Bonding
20. Leadframe: a. Paddle/flag material: b. Paddle/flag width (mils): c. Paddle/flag length (mils): d. Paddle/flag plating: e. Paddle/flag plating thickness (μm): f. Finger material: g. Finger plating: h. Finger plating thickness (μm): i. Lead material: j. Lead plating: k. Lead plating thickness (μm):	 Copper, 68*94mils NiPdAu See 20a See 20a See 20a NiPdAu / 0.5μm min Copper See 20a 5μm min Copper See 20a 0.5μm min
21. Unpackaged Die (if not packaged): a. Cap metal composition: b. Size of cap metal: c. Bump composition: d. Ball size:	 N/A N/A N/A N/A
22. Header Material:	N/A
23. Thermal Resistance: a. θ_{JA} °C/W (approx): b. θ_{JC} °C/W (approx): c. Special thermal dissipation construction techniques	 190 39 N/A
24. Test circuits, bias(es), & operational conditions imposed during the supplier's life and environmental tests:	Reliability test circuit figures attached (see appendix) ☐
25. Fault Grade Coverage (%)	N/A (not digital circuitry)

Attachments: Die Photo Package Outline Drawing Die Cross-section Drawing Wire & Die Placement Diagram Test Circuits, Bias Levels, & Conditions	 ☒ ☒ See data sheet See 11 See § 18 See 24	Requirements: 1. A separate Design, Construction & Qualification must be submitted for each P/N, wafer fab, and Assembly location. 2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below.

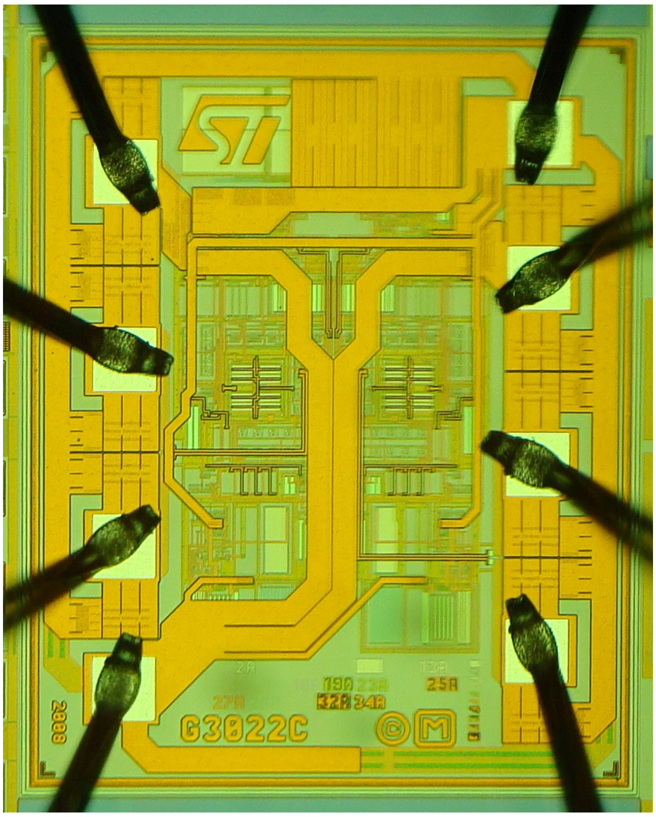
Completed by:		Certified by:
Typed/Printed:	Electronic qualification report	Electronic qualification report
Signature:	See approval list	See approval list
Title:	Product Engineer	Product Engineering & Product Quality Manager

Page 2 of 3 AEC-Q100 CofDC 6/03

Mask steps description

MASK LEVEL REFERENCE	DESCRIPTION
28	N BURIED
29	P BURIED
24	N ISOLATION
02	ACTIVE
01	N WELL
04	N+ SINKER
08	P WELL
26	PRESIST
13	POLY 1
05	P LDD
09	P BASE
14	N LDD
16	N+
17	P+
18	SIPROT
19	CONTACT
23	METAL 1
25	VIA 1
27	METAL 2
32	VIA 2
34	METAL 3
31	PASSIVATION
50	N BASE

Die photo



Q100 Certification of Design, Construction and Qualification

Supplier Name: ST Microelectronics
Supplier Part Number: TS3022ID/IDT

Item Name	Supplier Response
1. User's Part Number:	TS3022ID / IDT
2. Supplier's Part Number/Data Sheet:	TS3022ID / IDT / CD00222487
3. Die Fab Facility & Process ID:	UMC & HF5CMOS-AF30
4. Assembly Facility & Process ID:	BOUSKOURA B/E & 7861402
5. Final Quality Control A (Test) Facility:	BOUSKOURA B/E
6. Die: a. Die family: b. Die mask set revision & name:	 N/A 3022CA
7. Die Technology Description: a. Die channel length: b. Die gate length: c. Die process technology: d. Die supplier process ID (Mask #): e. Number of transistors or gates: f. Number of mask steps:	 N/A N/A HF5CMOS HF5CMOS-AF30 N/A 23
8. Die Dimensions: a. Die width: b. Die length: c. Die thickness:	 920 micron 750 micron 280 micron
9. Die Metallization: a. Die metallization material(s): b. Number of layers: c. Thickness (per layer): d. % of alloys (if present):	 AlCu/TinArc - AlCu/TinArc - AlCu/TinArc 3 0.55 micron / 0.55 micron / 0.85 micron N/A
10. Die Passivation: a. Number of passivation layers: b. Die passivation material(s): c. Thickness(es) & tolerances:	 See 10b. PSG + NITRIDE N/A
11. Pictorial Cross-Section:	See attached ☐ Not available ☒
12. Die Prep Backside: a. Die prep method: b. Die metallization: c. Thickness(es) & tolerances:	 See 12b. LAPPED SILICON N/A
13. Die Separation Method (Kerf Depth):	100% Sawing
14. Die Attach: a. Die attach material ID: b. Die attach method:	 GLUE HITACHI EN4900 ST10 10ml/25g Sy Epoxy glue
15. Package: a. Type of package: b. Ball/lead count:	 SO 08 .15 JEDEC See 15a.
16. Mold Compound: a. Mold compound supplier & ID: b. Flammability rating: c. Mold compound type: d. MSL level (if known):	 RESIN NITTO MP8000CH4-2A D14mm W3.5g UL 94 V1 ☐ UL 94 V0 ☒ Epoxy 1

17. Wire Bond: a. Wire bond material: b. Wire bond diameter (mils):	 WIRE Au D1 BL9-12g EL3-6% sp2x2' 2000m 1
18. Wire Bond Diagram:	Bonding diagram reference : 7757467 attached ☐
19. Wire Bond: a. Type of wire bond at die: b. Type of wire bond at leadframe:	 Ball Bonding Stitch Bonding
20. Leadframe: a. Paddle/flag material: b. Paddle/flag width (mils): c. Paddle/flag length (mils): d. Paddle/flag plating: e. Paddle/flag plating thickness (μm): f. Finger material: g. Finger plating: h. Finger plating thickness (μm): i. Lead material: j. Lead plating: k. Lead plating thickness (μm):	 Copper, 85*85mils NiPdAu See 20a See 20a See 20a NiPdAu / 0.5μm min Copper See 20a 5μm min Copper NiPdAu 0.5μm min
21. Unpackaged Die (if not packaged): a. Cap metal composition: b. Size of cap metal: c. Bump composition: d. Ball size:	 N/A N/A N/A N/A
22. Header Material:	N/A
23. Thermal Resistance: a. θ_{JA} °C/W (approx): b. θ_{JC} °C/W (approx): c. Special thermal dissipation construction techniques	 85 30 N/A
24. Test circuits, bias(es), & operational conditions imposed during the supplier's life and environmental tests:	Reliability test circuit figures attached (see appendix) ☐
25. Fault Grade Coverage (%)	N/A (not digital circuitry)

<u>Attachments:</u>

Die Photo	☒
Package Outline Drawing	☒ See data sheet
Die Cross-section Drawing	See 11
Wire & Die Placement Diagram	See § 18
Test Circuits, Bias Levels, & Conditions	See 24

<u>Requirements:</u>

1. A separate Design, Construction & Qualification must be submitted for each P/N, wafer fab, and Assembly location.

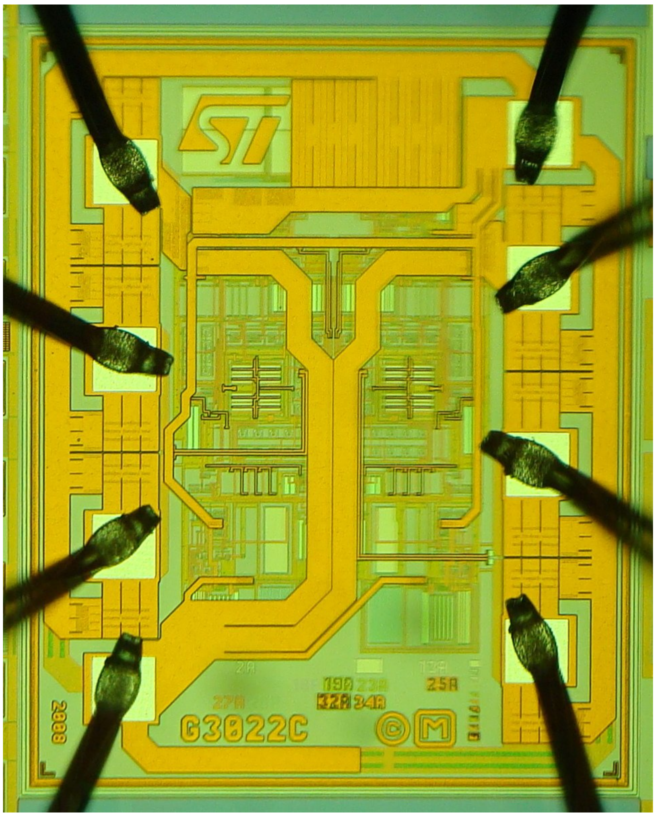
2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below.

Completed by:		Certified by:
Typed/Printed:	Electronic qualification report	Electronic qualification report
Signature:	See approval list	See approval list
Title:	Product Engineer	Product Engineering & Product Quality Manager

Mask steps description

MASK LEVEL REFERENCE	DESCRIPTION
28	N BURIED
29	P BURIED
24	N ISOLATION
02	ACTIVE
01	N WELL
04	N+ SINKER
08	P WELL
26	PRESIST
13	POLY 1
05	P LDD
09	P BASE
14	N LDD
16	N+
17	P+
18	SIPROT
19	CONTACT
23	METAL 1
25	VIA 1
27	METAL 2
32	VIA 2
34	METAL 3
31	PASSIVATION
50	N BASE

Die photo



3. Detailed Results of Qualification

3.1. Electrical Characterization & Test diagrams & Cpk

Data Sheet / Customer Specification

Extract from TEI specification

STMicroelectronics-APM Group -AMPS Business Unit

Product Line: **302201**

Description: **Dual rail to rail 1.8V high speed micropower comparator**

Product name: **TS3022**

Note:
Temperature:T for full temperature range
Operator: * for all operators;
A for operator A...
Guarantee:
T for tested in production
P for testable on automatic tester
C for tested by correlation
D for guarantee by design (not testable)
E for evaluated during the qualification

DOCUMENT INFORMATION

Approval history

Revision 3

Activated on: Aug/24/2009 New Vio limits for cut 3.0
Initiated by: BATEK Miroslav

Signator	Function	Approved on
CHASSAGNEUX Alain	Pdt Eng. manager	Aug/17/2009
BANCHERI Nathalie	P.Eng. team manager	Aug/19/2009
SMAT Radim	Busin. dev. engineer	Aug/17/2009
ZNOJEMSKY Karel	Designer	Aug/17/2009
BATEK Miroslav	Product engineer	Aug/17/2009

Revision 2

Activated on: Aug/28/2006 New version in line with single comp 3021.
Initiated by: BATEK Miroslav

Signator	Function	Approved on
CHASSAGNEUX Alain	Pdt Eng. manager	Aug/21/2006
PONTAROLLO Serge	Designer	Aug/25/2006
SVRCEK Jiri	Designer	Aug/18/2006
REPELLIN Stephane	Product responsible	Aug/21/2006
BATEK Miroslav	Product engineer	Aug/18/2006
ZNOJEMSKY Karel	Designer	Aug/21/2006
SMAT Radim	Busin. dev. engineer	Aug/18/2006
MIKOTA Jan	Product Responsible	Aug/18/2006
D'AGOSTINO Jerome	Busin. dev. engineer	Aug/28/2006
BANCHERI Nathalie	P.Eng. team manager	Aug/18/2006

TABLE OF CONTENTS

1. Parameters / Conditions

Parameter: **AMR** - *Absolute maximum ratings* — Test diagram: **T115A**

Oper.	Vers.	Test conditions	T°C	Limits (Unit: N/A) min	typical	max	Guar.
A	1	Vccp_V 5.50; Vccn_V 0.00; Vid_V 5.50; Vicp_V 5.50; Vicn_V -0.30; VccpM_V 5.50; VccnM_V 0.00; IoM N/A; Vstby_V N/A	25				T

Parameter: **CMR** - *Common mode ratio* — Test diagram: **T109A**

Oper.	Vers.	Test conditions	T°C	Limits (Unit: dB) min	typical	max	Guar.
A	80	Vccp_V 2.00; Vccn_V 0.00; Vic_V 0.00; dVic_V 2.00; Vro_V 0.70; VRL_V N/A; RL_Kohm No load	25	48.00	67.00		T
A	91	Vccp_V 3.30; Vccn_V 0.00; Vic_V 0.00; dVic_V 3.30; Vro_V 0.70; VRL_V N/A; RL_Kohm No load	25	50.00	75.00		T
A	100	Vccp_V 5.00; Vccn_V 0.00; Vic_V 0.00; dVic_V 5.00; Vro_V 1.40; VRL_V N/A; RL_Kohm No load	25	52.00	79.00		T

Parameter: **DVio** - *Input offset voltage drift* — Test diagram: **T107A**

Oper.	Vers.	Test conditions	T°C	Limits (Unit: µV/°C) min	typical	max	Guar.
A	105	Tmin_?C -40.00; Tmax_?C 125.00; Iset_?A N/A; Vset_V N/A	T		3.00	20.00	T

Parameter: **Iccn** - *Negative supply current per operator* — Test diagram: **T106C**

Oper.	Vers.	Test conditions	T°C	Limits (Unit: µA) min	typical	max	Guar.
A	27	Vccp_V 2.00; Vccn_V 0.00; Vid_V -0.20; Vin_V 0.00; *Vicm=0V, Out=L*	25		84.00	105.00	T
A	27	Vccp_V 2.00; Vccn_V 0.00; Vid_V -0.20; Vin_V 0.00; *Vicm=0V, Out=L*	T			125.00	T
A	32	Vccp_V 3.30; Vccn_V 0.00; Vid_V -0.20; Vin_V 0.00; *Vicm=0V, Out=L*	25		86.00	110.00	T
A	32	Vccp_V 3.30; Vccn_V 0.00; Vid_V -0.20; Vin_V 0.00; *Vicm=0V, Out=L*	T			125.00	T
A	51	Vccp_V 5.00; Vccn_V 0.00; Vid_V -0.20; Vin_V 0.00; *Vicm=0V, Out=L*	25		89.00	115.00	T
A	51	Vccp_V 5.00; Vccn_V 0.00; Vid_V -0.20; Vin_V 0.00; *Vicm=0V, Out=L*	T			135.00	T

Parameter: **Iccp** - *Positive supply current per operator* — Test diagram: **T106C**

Oper.	Vers.	Test conditions	T°C	Limits (Unit: µA) min	typical	max	Guar.
A	81	Vccp_V 2.00; Vccn_V 0.00; Vid_V 0.20; Vin_V 0.00; *Vicm=0V, Out=H*	25		73.00	90.00	T

Oper.	Vers.	Test conditions	T°C	min	typical	max	Guar.
A	81	Vccp_V 2.00, Vccn_V 0.00, Vid_V 0.20, Vin_V 0.00 — *Vicm=0V, Out=H*	T			115.00	T
A	83	Vccp_V 3.30, Vccn_V 0.00, Vid_V 0.20, Vin_V 0.00 — *Vicm=0V, Out=H*	25		75.00	90.00	T
A	83	Vccp_V 3.30, Vccn_V 0.00, Vid_V 0.20, Vin_V 0.00 — *Vicm=0V, Out=H*	T			120.00	T
A	85	Vccp_V 5.00, Vccn_V 0.00, Vid_V 0.20, Vin_V 0.00 — *Vicm=0V, Out=H*	25		77.00	95.00	T
A	85	Vccp_V 5.00, Vccn_V 0.00, Vid_V 0.20, Vin_V 0.00 — *Vicm=0V, Out=H*	T			125.00	T

Parameter: **Iib** - *Input bias current* Test diagram: **T103B**

Unit: nA

Oper.	Vers.	Vccp_V	Vic_V	RL_ohm	T°C	min	typical	max	Guar.
A	88	2.00	0.50		25	-160.00	-86.00	160.00	T
A	88	2.00	0.50		T	-300.00		300.00	T
A	89	3.30	0.50		25	-160.00	-86.00	160.00	T
A	89	3.30	0.50		T	-300.00		300.00	T
A	90	5.00	0.50		25	-160.00	-86.00	160.00	T
A	90	5.00	0.50		T	-300.00		300.00	T

Parameter: **Iio** - *Input offset current* Test diagram: **T101A**

Unit: nA

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vro_V	VRL_V	RL_Kohm	Vstby_V	T°C	min	typical	max	Guar.
A	102	2.00	0.00	0.50	N/A	N/A	No load	N/A	25	-20.00	1.00	20.00	T
A	102	2.00	0.00	0.50	N/A	N/A	No load	N/A	T	-100.00		100.00	T
A	103	3.30	0.00	0.50	N/A	N/A	No load	N/A	25	-20.00	1.00	20.00	T
A	103	3.30	0.00	0.50	N/A	N/A	No load	N/A	T	-100.00		100.00	T
A	104	5.00	0.00	0.50	N/A	N/A	No load	N/A	25	-20.00	1.00	20.00	T
A	104	5.00	0.00	0.50	N/A	N/A	No load	N/A	T	-100.00		100.00	T

Parameter: **SVR** - *Supply Voltage Rejection Ratio* Test diagram: **T105A**

Unit: dB

Oper.	Vers.	Vccp_V	Vccn_V	dVccp_V	dVccn_V	Vic_V	Vro_V	VRL_V	RL_Kohm	T°C	min	typical	max	Guar.
A	107	5.00	0.00	3.00	0.00	0.00	0.00	N/A	No load	25	58.00	73.00		T

Vcc=2-5V, Vicm=0V

Parameter: **Vio** - *Input offset voltage* Test diagram: **T101B**

Unit: mV

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vro_V	VRL_V	RL_Kohm	T°C	min	typical	max	Guar.
A	45	2.00	0.00	-0.20	0.70	N/A	No load	25	-6.00	0.50	6.00	T
A	45	2.00	0.00	-0.20	0.70	N/A	No load	T	-7.00		7.00	T
A	46	2.00	0.00	0.00	0.70	N/A	No load	25	-6.00	0.50	6.00	T
A	46	2.00	0.00	0.00	0.70	N/A	No load	T	-7.00		7.00	T
A	47	2.00	0.00	1.00	0.70	N/A	No load	25	-6.00	0.50	6.00	T
A	47	2.00	0.00	1.00	0.70	N/A	No load	T	-7.00		7.00	T
A	48	2.00	0.00	2.00	0.70	N/A	No load	25	-6.00	0.50	6.00	T
A	48	2.00	0.00	2.00	0.70	N/A	No load	T	-7.00		7.00	T
A	49	2.00	0.00	2.20	0.70	N/A	No load	25	-6.00	0.50	6.00	T
A	49	2.00	0.00	2.20	0.70	N/A	No load	T	-7.00		7.00	T
A	50	3.30	0.00	-0.20	0.70	N/A	No load	25	-6.00	0.20	6.00	T
A	50	3.30	0.00	-0.20	0.70	N/A	No load	T	-7.00		7.00	T
A	52	3.30	0.00	0.00	0.70	N/A	No load	25	-6.00	0.20	6.00	T
A	52	3.30	0.00	0.00	0.70	N/A	No load	T	-7.00		7.00	T
A	53	3.30	0.00	1.65	0.70	N/A	No load	25	-6.00	0.20	6.00	T
A	53	3.30	0.00	1.65	0.70	N/A	No load	T	-7.00		7.00	T
A	54	3.30	0.00	3.30	0.70	N/A	No load	25	-6.00	0.20	6.00	T
A	54	3.30	0.00	3.30	0.70	N/A	No load	T	-7.00		7.00	T
A	55	3.30	0.00	3.50	0.70	N/A	No load	25	-6.00	0.20	6.00	T
A	55	3.30	0.00	3.50	0.70	N/A	No load	T	-7.00		7.00	T
A	56	5.00	0.00	-0.20	1.40	N/A	No load	25	-6.00	0.20	6.00	T
A	56	5.00	0.00	-0.20	1.40	N/A	No load	T	-7.00		7.00	T
A	57	5.00	0.00	0.00	1.40	N/A	No load	25	-6.00	0.20	6.00	T
A	57	5.00	0.00	0.00	1.40	N/A	No load	T	-7.00		7.00	T
A	58	5.00	0.00	2.50	1.40	N/A	No load	25	-6.00	0.20	6.00	T
A	58	5.00	0.00	2.50	1.40	N/A	No load	T	-7.00		7.00	T

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vro_V	VRL_V	RL_Kohm	T°C	min	typical	max	Guar.
A	59	5.00	0.00	5.00	1.40	N/A	No load	25	-6.00	0.20	6.00	T
A	59	5.00	0.00	5.00	1.40	N/A	No load	T	-7.00		7.00	T
A	60	5.00	0.00	5.20	1.40	N/A	No load	25	-6.00	0.20	6.00	T
A	60	5.00	0.00	5.20	1.40	N/A	No load	T	-7.00		7.00	T

Parameter: **Voh** - *High level output voltage* Test diagram: **T117B**

Unit: V

Oper.	Vers.	Vccp_V	Vccn_V	Vid_V	Vin_V	Ioh_mA	Iol_mA	T°C	min	typical	max	Guar.
A	64	2.00	0.00	1.00	1.00	-1.00	N/A	25	1.88	1.92		T
A	64	2.00	0.00	1.00	1.00	-1.00	N/A	T	1.80			T
A	65	2.00	0.00	1.00	1.00	-4.00	N/A	25	1.62	1.74		T
A	65	2.00	0.00	1.00	1.00	-4.00	N/A	T	1.50			T
A	66	3.30	0.00	1.00	1.65	-1.00	N/A	25	3.20	3.25		T
A	66	3.30	0.00	1.00	1.65	-1.00	N/A	T	3.10			T
A	67	3.30	0.00	1.00	1.65	-4.00	N/A	25	3.04	3.14		T
A	67	3.30	0.00	1.00	1.65	-4.00	N/A	T	2.95			T
A	68	5.00	0.00	1.00	2.50	-1.00	N/A	25	4.92	4.97		T
A	68	5.00	0.00	1.00	2.50	-1.00	N/A	T	4.85			T
A	69	5.00	0.00	1.00	2.50	-4.00	N/A	25	4.80	4.84		T
A	69	5.00	0.00	1.00	2.50	-4.00	N/A	T	4.70			T

Parameter: **Vol** - *Low level output voltage* Test diagram: **T117B**

Unit: V

Oper.	Vers.	Vccp_V	Vccn_V	Vid_V	Vin_V	Ioh_mA	Iol_mA	T°C	min	typical	max	Guar.
A	72	2.00	0.00	1.00	1.00	N/A	1.00	25		0.06	0.10	T
A	72	2.00	0.00	1.00	1.00	N/A	1.00	T			0.15	T
A	74	2.00	0.00	1.00	1.00	N/A	4.00	25		0.20	0.32	T
A	74	2.00	0.00	1.00	1.00	N/A	4.00	T			0.45	T
A	75	3.30	0.00	1.00	1.65	N/A	1.00	25		0.04	0.08	T
A	75	3.30	0.00	1.00	1.65	N/A	1.00	T			0.15	T
A	76	3.30	0.00	1.00	1.65	N/A	4.00	25		0.13	0.24	T
A	76	3.30	0.00	1.00	1.65	N/A	4.00	T			0.35	T

Oper.	Vers.	Vccp_V	Vccn_V	Vid_V	Vin_V	Ioh_mA	Iol_mA	T°C	min	typical	max	Guar.
A	77	5.00	0.00	1.00	2.50	N/A	1.00	25		0.03	0.08	T
A	77	5.00	0.00	1.00	2.50	N/A	1.00	T			0.15	T
A	78	5.00	0.00	1.00	2.50	N/A	4.00	25		0.13	0.18	T
A	78	5.00	0.00	1.00	2.50	N/A	4.00	T			0.25	T

Parameter: **tf** - *Fall time* Test diagram: **T130A**

Unit: ns

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vod_mV	f_KHz	VRL_V	RL_Kohm	CL_pF	T°C	min	typical	max	Guar.
A	4	2.00	0.00	-0.20	100.00	10.00	0.00	10.00	50.00	25		8.00		E
A	5	2.00	0.00	1.00	100.00	10.00	0.00	10.00	50.00	25		8.00		E
A	6	2.00	0.00	2.20	100.00	10.00	0.00	10.00	50.00	25		8.00		E
A	33	3.30	0.00	-0.20	100.00	10.00	0.00	10.00	50.00	25		5.00		E
A	34	3.30	0.00	1.65	100.00	10.00	0.00	10.00	50.00	25		5.00		E
A	35	3.30	0.00	3.50	100.00	10.00	0.00	10.00	50.00	25		5.00		E
A	36	5.00	0.00	-0.20	100.00	10.00	0.00	10.00	50.00	25		4.00		E
A	108	5.00	0.00	2.50	100.00	10.00	0.00	10.00	50.00	25		4.00		E
A	109	5.00	0.00	5.20	100.00	10.00	0.00	10.00	50.00	25		4.00		E

Parameter: **tphl** - *Response time high to low* Test diagram: **T130A**

Unit: ns

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vod_mV	f_KHz	VRL_V	RL_Kohm	CL_pF	T°C	min	typical	max	Guar.
A	12	2.00	0.00	0.00	20.00	10.00	0.00	0.00	50.00	25		49.00	75.00	T
A	14	3.30	0.00	0.00	20.00	10.00	0.00	0.00	50.00	25		51.00	80.00	T
A	17	5.00	0.00	0.00	20.00	10.00	0.00	0.00	50.00	25		55.00	95.00	T
A	24	2.00	0.00	0.00	100.00	10.00	0.00	0.00	50.00	25		38.00	60.00	T
A	26	3.30	0.00	0.00	100.00	10.00	0.00	0.00	50.00	25		41.00	65.00	T
A	29	5.00	0.00	0.00	100.00	10.00	0.00	0.00	50.00	25		45.00	75.00	T

Parameter: **tplh** - *response time low to high* Test diagram: **T130A**

Unit: ns

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vod_mV	f_KHz	VRL_V	RL_Kohm	CL_pF	T°C	min	typical	max	Guar.
A	12	2.00	0.00	0.00	20.00	10.00	0.00	0.00	50.00	25		38.00	75.00	T
A	14	3.30	0.00	0.00	20.00	10.00	0.00	0.00	50.00	25		42.00	85.00	T

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vod_mV	f_KHz	VRL_V	RL_Kohm	CL_pF	T°C	min	typical	max	Guar.
A	17	5.00	0.00	0.00	20.00	10.00	0.00	0.00	50.00	25		48.00	105.00	T
A	24	2.00	0.00	0.00	100.00	10.00	0.00	0.00	50.00	25		33.00	60.00	T
A	26	3.30	0.00	0.00	100.00	10.00	0.00	0.00	50.00	25		34.00	65.00	T
A	29	5.00	0.00	0.00	100.00	10.00	0.00	0.00	50.00	25		38.00	75.00	T

Parameter: **tr** - *Rise time* Test diagram: **T130A**

Unit: ns

Oper.	Vers.	Vccp_V	Vccn_V	Vic_V	Vod_mV	f_KHz	VRL_V	RL_Kohm	CL_pF	T°C	min	typical	max	Guar.
A	4	2.00	0.00	-0.20	100.00	10.00	0.00	10.00	50.00	25		9.00		E
A	5	2.00	0.00	1.00	100.00	10.00	0.00	10.00	50.00	25		9.00		E
A	6	2.00	0.00	2.20	100.00	10.00	0.00	10.00	50.00	25		9.00		E
A	33	3.30	0.00	-0.20	100.00	10.00	0.00	10.00	50.00	25		7.00		E
A	34	3.30	0.00	1.65	100.00	10.00	0.00	10.00	50.00	25		7.00		E
A	35	3.30	0.00	3.50	100.00	10.00	0.00	10.00	50.00	25		7.00		E
A	36	5.00	0.00	-0.20	100.00	10.00	0.00	10.00	50.00	25		4.00		E
A	37	5.00	0.00	2.50	-100.00	10.00	0.00	10.00	50.00	25		4.00		E
A	38	5.00	0.00	5.20	-100.00	10.00	0.00	10.00	50.00	25		4.00		E

2. Test diagrams

2.1. T101A

Vio : Input offset voltage (_mV _µV)

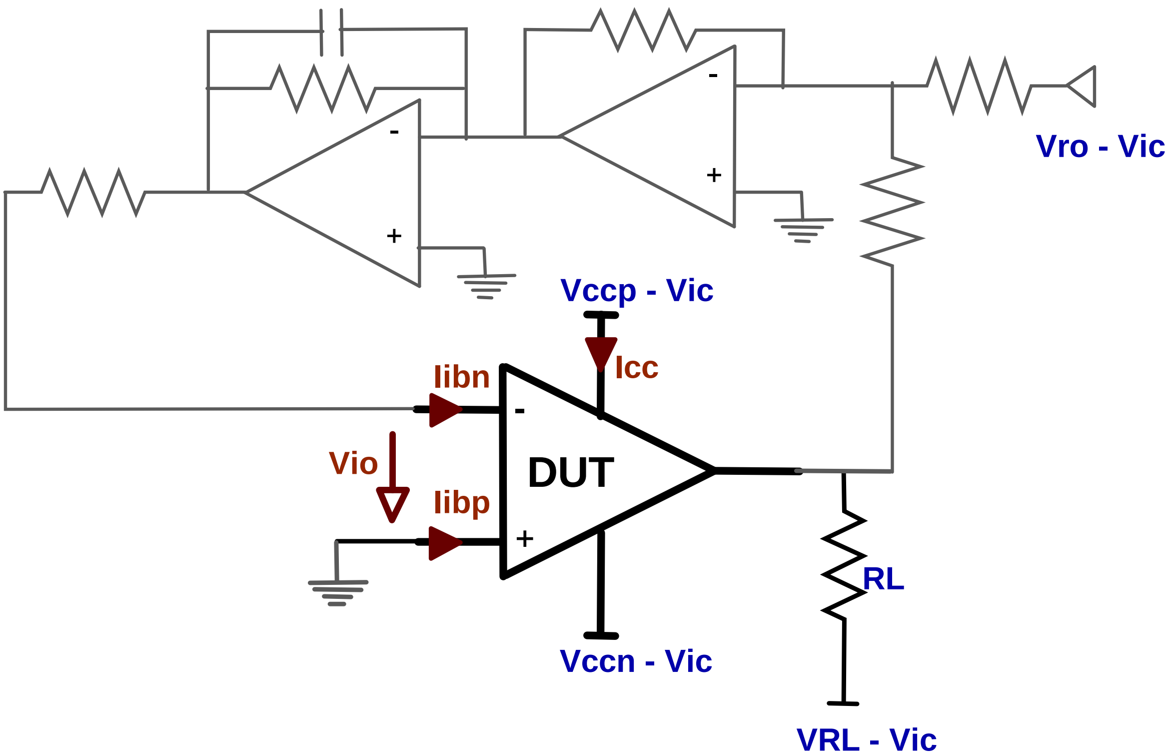
Icc : Supply current (_mA _µA)

Iio : Input offset current (_pA _nA _µA _mA)

Iio = Iibn - Iibp

Iib : Input bias current (_pA _nA _µA _mA)

Iibp (non_inverting); Iibn (inverting)



Vccp_V : positive supply voltage

Vccn_V : negative supply voltage

Vic_V : common mode input voltage

Vro_V : Op_amp loop input voltage

VRL_V : load reference voltage (N/A if not defined)

RL_Kohm: load resistor (no load if not defined)

Vstby_V : Stand-by voltage (N/A)

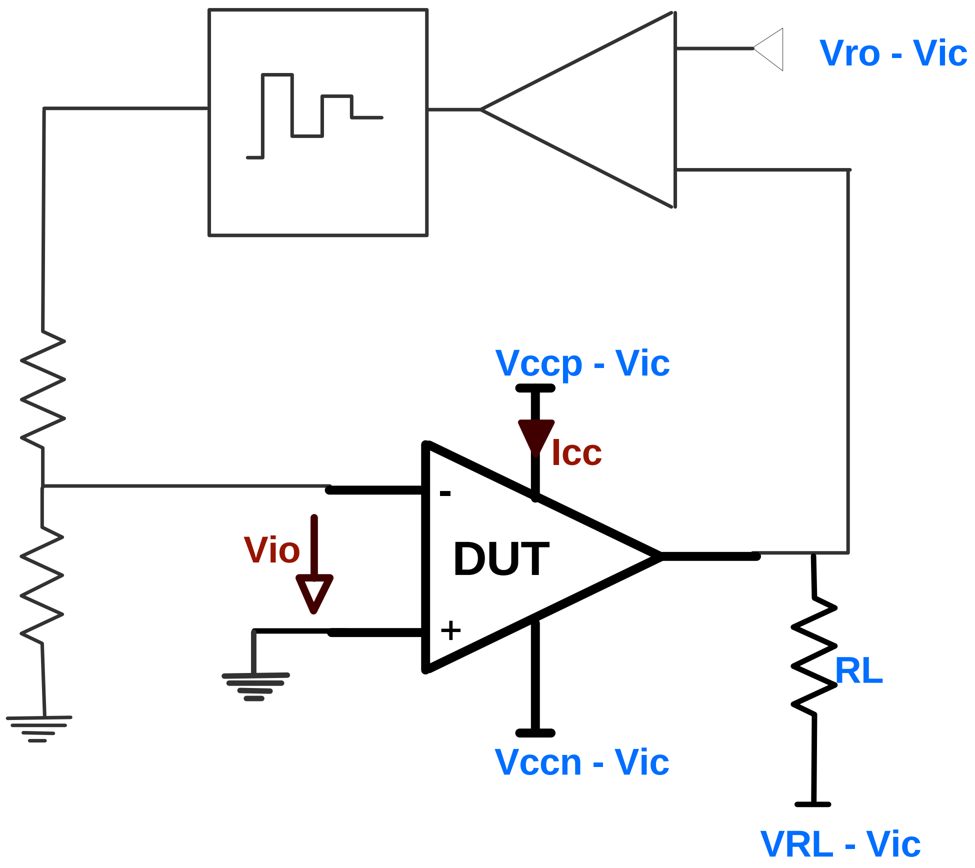
DUT : device under test

T101A_1

2.2. T101B

Vio : Input offset voltage (_mV _µV)

Icc : Supply current (_mA _µA)



Vccp_V : positive supply voltage

Vccn_V : negative supply voltage

Vic_V : common mode input voltage

Vro_V : Op_amp loop input voltage

VRL_V : load reference voltage (N/A if not defined)

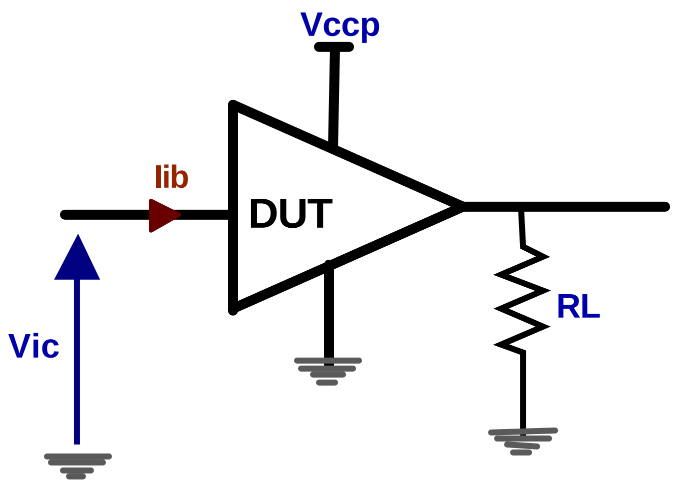
RL_Kohm: load resistor (no load if not defined)

DUT : device under test

T101B_1

2.3. T103B

Iib : Input bias current (_pA _nA _µA _mA)



Vccp_V : Supply voltage

Vic_V : common mode input voltage

RL_ohm: load resistor (no load if not defined)

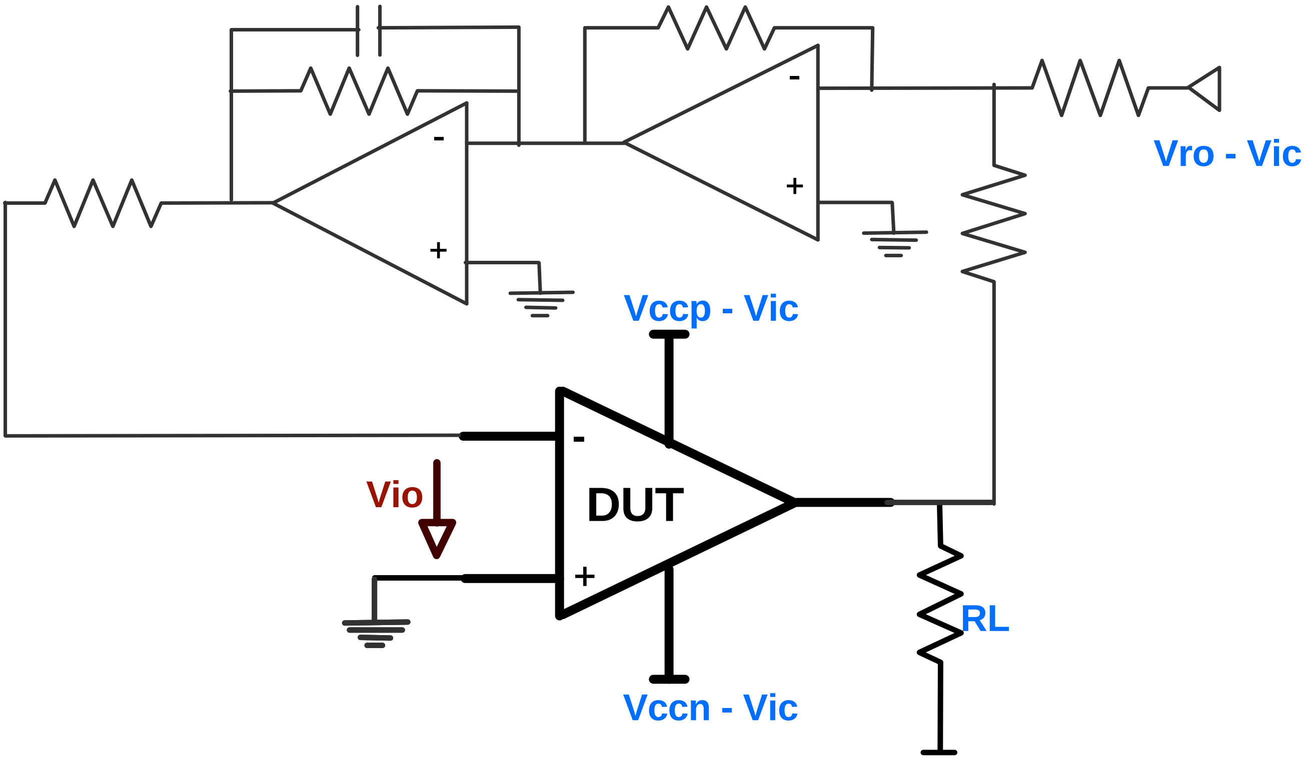
DUT : device under test

T103B_1

2.4. T105A

SVR : Supply voltage rejection ratio (_dB)

SVR = 20 * log |d(Vccp-Vccn) / dVio|



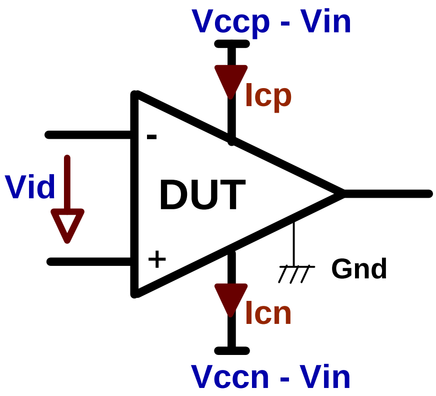
Vccp_V : positive supply voltage ;initial value
Vccn_V : negative supply voltage ; initial value
dVccp_V : positive supply voltage variation
dVccn_V : negative supply voltage variation
Vic_V : common mode input voltage
Vro_V : Op_amp loop input voltage
VRL_V : load reference voltage(N/A if not defined)
RL_Kohm : load resistor (no load if not defined)

DUT : device under test

T105A_1

2.5. T106C

Icp: Positive supply current per operator(_mA_uA)
Icn: Negative supply current per operator(_mA_uA)



Vccp_V : positive supply voltage

Vccn_V : negative supply voltage

Vid_V : differential input voltage

Vin_V : inverting input voltage

T106C_1

2.6. T107A

D... + parameter code... (unit = _parameter unit for absolute drift)
_parameter unit/°C for drift per °C)
_% for drift divided per initial value)

Drift between Tmin_°C and Tmax_°C
(see Temperature range if not defined)

T107A_1

2.7. T108A

S... + parameter code ... :(unit = _parameter unit for absolute drift)
_parameter unit/h for drift per hours)
_% for drift divided per initial value)

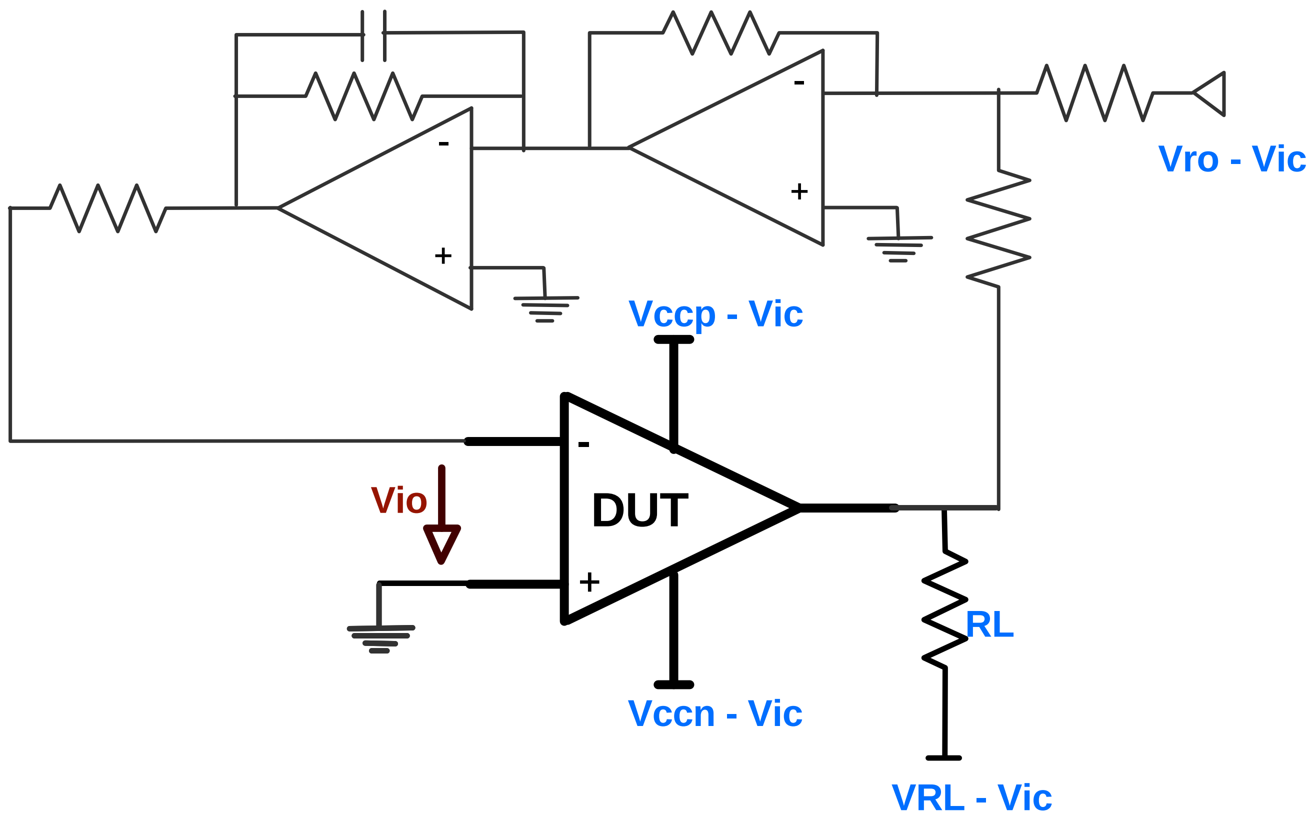
Drift between time1_h and time2_h

T108A_1

2.8. T109A

CMR : Common mode voltage rejection ratio (_dB)

CMR = 20 * log |dVic / dVio|



Vccp_V : Positive supply voltage

Vccn_V : Negative supply voltage

Vic_V : Common mode input voltage ; initial value

dVic_V : Common mode input voltage variation

Vro_V : Op_amp loop input voltage

VRL_V : Load reference voltage (N/A if not defined)

RL_Kohm : Load resistor (no load if not defined)

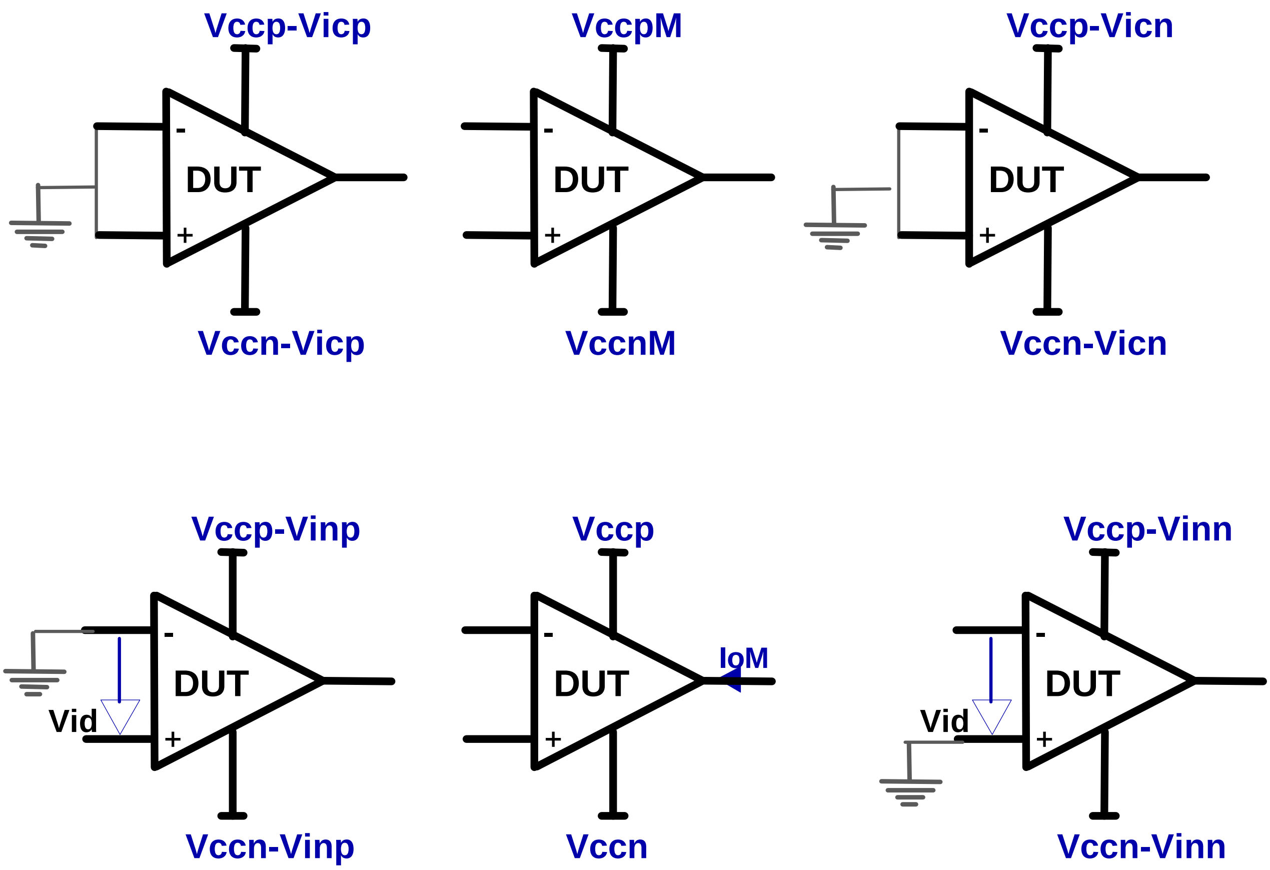
DUT : device under test

T109A_1

2.9. T115A

AMR : Absolute maximum ratings

No measure (N/M)



Vccp_V : positive supply voltage
Vccn_V : negative supply voltage
Vinp_V : inverting input voltage for VidM>0
Vinn_V : inverting input voltage for VidM<0
Vid_V : differential input voltage
Vicp_V : common mode input voltage for Vic>0
Vicn_V : common mode input voltage for Vic<0
VccpM_V : maximun positive supply voltage
VccnM_V : minimun negative supply voltage
IoM : maximum output current (_mA)
Vstby_V : Stand-by voltage (N/A)

DUT : device under test

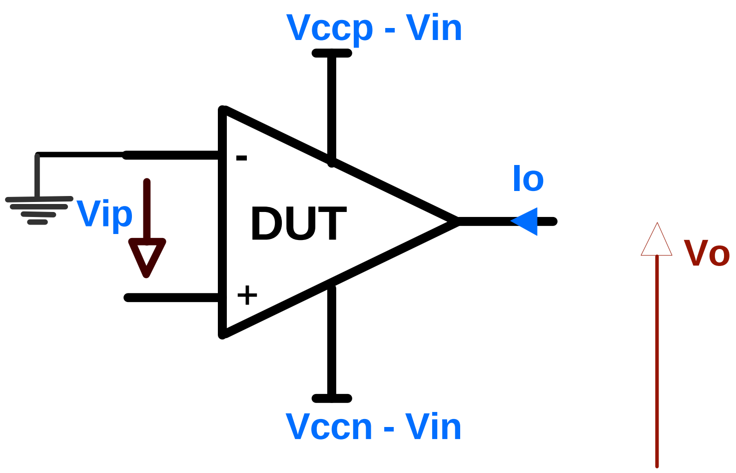
T115A_1

2.10. T117B

Output voltage (_V)

Voh : high level

Vol : low level



Vccp_V : positive supply voltage

Vccn_V : negative supply voltage

Vid_V : differential input voltage |Vip|

(Vip = Vid for Voh; Vip = -Vid for Vol)

Vin_V : inverting input voltage

Ioh_mA : output current (Io) for Voh (N/A for Vol)

Iol_mA : output current (Io) for Vol (N/A for Voh)

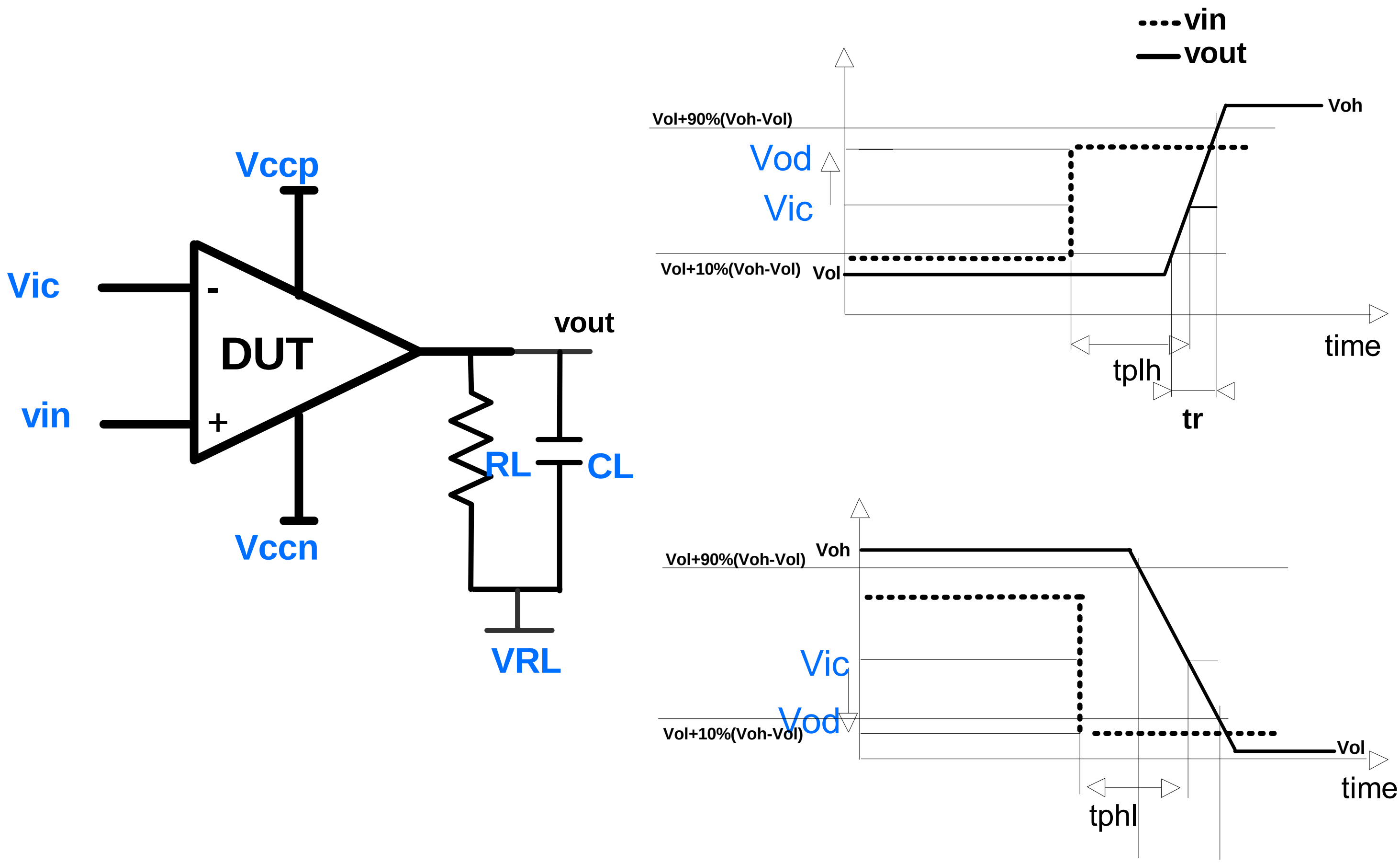
DUT : device under test

T117B_1

2.11. T130A

tr : rise time (_uS _nS)
tf : fall time (_uS _nS)

tplh : response time low to high
tphl : response time high to low



Vccp_V : positive supply voltage (Vcc+)

Vccn_V : negative supply voltage (Vcc-)

Vic_V : reference input voltage (V ref)

Vod_mV : over drive level voltage (TTL if not defined) Vod_mV>0 for tplh, Vod_mV<0 for tphl

f_KHz : frequency

VRL_V : Load reference (N/A if no load)

RL_Kohm : load resistor (no load if not defined)

CL_pF: load capacitor no loadf not defined)

DUT : device under test

T130A_1

Here are the statistical distributions for each electrical parameter versus datasheet specification.
These results conform to ST mat30 standard results.
All statistical data are showed separately for comp A and comp B in the same package.

[EWS]

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Vio [mV]	2	-0.2			-6	6	-2.81	-2.28	2.17	2.37	-0.47	-0.41	0.64	0.64	2.87	2.91
		0					-2.76	-2.63	2.21	2.37	-0.47	-0.41	0.64	0.64	2.88	2.92
		1					-3.48	-2.68	4.18	3.34	-0.31	-0.26	0.83	0.83	2.29	2.29
		2					-2.71	-2.49	4.27	4.51	0.67	0.66	0.90	0.90	1.97	1.97
		2.2					-2.44	-2.18	4.24	4.51	0.67	0.66	0.90	0.90	1.97	1.97
	3.3	-0.2					-2.79	-2.33	2.43	2.59	-0.18	-0.12	0.66	0.65	2.96	3.01
		0					-2.64	-2.05	2.42	2.62	-0.18	-0.12	0.65	0.65	2.97	3.02
		1.65					-2.70	-2.34	2.45	2.63	-0.18	-0.13	0.66	0.65	2.95	3.00
		3.3					-2.73	-2.53	3.60	3.89	0.21	0.20	0.86	0.86	2.24	2.25
		3.5					-2.76	-2.15	3.62	3.90	0.21	0.20	0.86	0.86	2.24	2.24
	5	-0.2					-2.49	-1.88	2.81	2.91	0.19	0.24	0.66	0.65	2.92	2.93
		0					-2.51	-1.86	2.82	2.89	0.19	0.24	0.66	0.65	2.93	2.94
		2.5					-2.51	-2.17	2.82	2.93	0.19	0.24	0.67	0.66	2.89	2.90
		5					-2.81	-2.84	3.31	3.35	-0.15	-0.16	0.82	0.82	2.38	2.37
		5.2					-2.95	-2.72	3.33	3.33	-0.15	-0.16	0.82	0.82	2.38	2.37

Cpk < 2: Comparators team agreed with this Cpk to have more competitive Vio limits.

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min	max	avg	stdev	cpk
Icc [uA]	2.0	0.0	H			90.0	70.4	79.4	74.0	1.2	4.4
			L			105.0	81.2	92.5	85.3	1.5	4.5
		2.0	H			135.0	97.3	111.9	102.2	1.9	5.6
			L			120.0	87.0	100.1	91.5	1.7	5.5
	3.3	0.0	H			90.0	72.3	81.0	75.7	1.2	3.9
			L			110.0	83.6	95.3	87.7	1.5	5.0
		3.3	H			140.0	100.3	115.7	105.5	2.0	5.7
			L			125.0	89.4	102.9	93.9	1.8	5.9
	5.0	0.0	H			95.0	74.1	83.4	77.8	1.2	4.6
			L			115.0	86.1	98.2	90.5	1.5	5.3
		5.0	H			145.0	103.9	120.0	109.1	2.1	5.7
			L			125.0	91.7	106.0	96.7	1.8	5.2

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Iib [nA]	2				-160	160	-120.6	-119.1	-87.0	-87.4	-97.6	-97.9	3.7	3.8	5.7	5.5
	3.3						-121.1	-119.6	-87.4	-87.8	-98.0	-98.3	3.7	3.8	5.6	5.4
	5						-121.4	-120.1	-87.7	-88.1	-98.4	-98.6	3.7	3.8	5.6	5.4
Iio [nA]	2				-20	20	0.01	0.59	2.07	4.42	0.38	2.48	0.29	0.47	22.50	12.4
	3.3						0.01	0.45	1.99	4.43	0.39	2.44	0.29	0.47	22.41	12.4
	5						0.01	0.57	2.08	4.42	0.39	2.46	0.29	0.47	22.33	12.3

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
CMRR [dB]	2				48		51.5	53.2	126.0	126.0	66.7	67.2	9.0	9.4	N/A	N/A
	3.3				50		57.5	59.7	130.4	130.4	75.0	75.2	9.8	9.7	N/A	N/A
	5				52		61.6	62.2	134.0	134.0	78.9	78.8	9.5	9.7	N/A	N/A
SVR [dB]					58		59.7	64.0	83.6	84.6	73.0	73.1	1.3	1.2	N/A	N/A

N/A ... CMRR and SVR in dB have not Normal (Gaussian) distribution

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Voh Vol [V]	2		H	1	1.88		1.92	1.92	1.93	1.93	1.92	1.92	0.00	0.00	12.4	11.6
			L			0.10	0.06	0.06	0.07	0.07	0.06	0.06	0.00	0.00	9.3	9.0
	3.3		H	1	3.20		3.25	3.25	3.26	3.26	3.25	3.25	0.00	0.00	18.7	16.9
			L			0.08	0.04	0.04	0.05	0.05	0.04	0.04	0.00	0.00	10.3	9.6
	5		H	4	4.80		4.82	4.83	4.85	4.86	4.84	4.84	0.00	0.00	4.5	4.0
			L			0.18	0.13	0.13	0.16	0.16	0.14	0.14	0.00	0.00	2.6	2.5

% of test with Cpk > 2:	94.9%
% of test with Cpk > 1.67:	100.0%
% of test with Cpk > 1.33:	100.0%

Here are the statistical distributions for each electrical parameter versus datasheet specification.
These results conform to ST mat30 standard results.
All statistical data are showed separately for comp A and comp B in the same package.

[FT Ambient Temerature]

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Vio [mV]	2	-0.2			-6	6	-2.47	-2.51	1.66	1.61	-0.53	-0.39	0.64	0.66	2.86	2.84
		0					-2.38	-2.22	1.62	1.60	-0.53	-0.39	0.63	0.65	2.90	2.86
		1					-2.69	-2.75	2.89	2.70	-0.35	-0.18	0.86	0.92	2.18	2.12
		2					-2.04	-2.16	3.46	3.88	0.66	0.65	0.99	0.95	1.79	1.87
		2.2					-2.68	-2.16	3.48	3.88	0.66	0.64	1.00	0.96	1.78	1.87
	3.3	-0.2					-2.23	-2.28	1.93	1.89	-0.23	-0.08	0.63	0.66	3.03	3.01
		0					-2.38	-1.93	1.93	1.88	-0.23	-0.08	0.64	0.65	3.00	3.03
		1.65					-2.14	-2.28	1.94	1.90	-0.23	-0.09	0.64	0.66	3.00	2.99
		3.3					-3.18	-2.30	2.96	3.33	0.21	0.19	0.96	0.92	2.02	2.11
		3.5					-2.99	-2.31	2.97	3.33	0.21	0.19	0.96	0.92	2.01	2.11
	5	-0.2					-1.86	-1.92	2.28	2.25	0.15	0.29	0.64	0.65	3.06	2.92
		0					-2.00	-1.92	2.28	2.26	0.16	0.29	0.62	0.65	3.12	2.94
		2.5					-2.02	-1.95	2.30	2.29	0.15	0.29	0.64	0.66	3.06	2.88
		5					-2.63	-2.68	2.51	2.91	-0.14	-0.18	0.91	0.90	2.15	2.16
		5.2					-2.76	-2.79	2.51	2.89	-0.13	-0.18	0.90	0.89	2.16	2.17

Cpk < 2: Comparators team agreed with this Cpk to have more competitive Vio limits.

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min	max	avg	stdev	cpk
Icc [uA]	2.0	0.0	H			90.0	70.0	80.8	74.0	1.4	3.9
			L			105.0	79.9	93.3	85.3	1.7	3.9
		2.0	H			135.0	96.2	113.7	102.1	2.2	5.0
			L			120.0	86.4	101.7	91.5	2.0	4.9
	3.3	0.0	H			90.0	72.0	82.9	76.1	1.4	3.3
			L			110.0	82.5	96.2	88.0	1.7	4.2
		3.3	H			140.0	99.7	117.8	105.7	2.3	5.0
			L			125.0	89.1	104.7	94.3	2.0	5.1
	5.0	0.0	H			95.0	74.0	85.1	78.2	1.4	4.0
			L			115.0	85.2	99.3	90.9	1.8	4.5
		5.0	H			145.0	103.1	121.9	109.3	2.4	5.0
			L			125.0	91.8	107.7	97.0	2.0	4.6

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Iib [nA]	2				-160	160	-124.3	-128.3	-92.5	-96.1	-103.3	-103.3	3.9	3.9	4.8	4.8
	3.3						-124.8	-128.7	-92.9	-96.5	-103.8	-103.8	3.9	3.9	4.8	4.8
	5						-125.3	-129.0	-93.3	-96.9	-104.1	-104.1	4.0	3.9	4.7	4.7
Iio [nA]	2				-20	20	0.01	0.01	3.17	3.58	0.64	1.04	0.48	0.64	13.49	9.8
	3.3						0.01	0.01	3.15	3.49	0.63	1.00	0.48	0.64	13.57	9.9
	5						0.01	0.01	3.27	3.58	0.65	1.01	0.49	0.64	13.17	9.9

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
CMRR [dB]	2				48		52.0	53.7	126.0	115.3	66.7	67.4	9.3	9.5	N/A	N/A
	3.3				50		58.3	59.9	123.8	130.4	74.1	74.6	9.2	9.4	N/A	N/A
	5				52		63.7	63.4	134.0	134.0	78.3	78.3	9.4	9.8	N/A	N/A
SVR [dB]					58		60.0	64.7	78.0	77.6	72.8	73.0	1.5	1.2	N/A	N/A

N/A ... CMRR and SVR in dB have not Normal (Gaussian) distribution

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Voh Vol [V]	2		H	1	1.88		1.92	1.92	1.93	1.93	1.92	1.92	0.00	0.00	11.88	12.7
			L			0.10	0.06	0.06	0.06	0.06	0.06	0.06	0.00	0.00	19.33	19.8
	3.3		H	1	3.20		3.25	3.25	3.25	3.25	3.25	3.25	0.00	0.00	24.70	25.5
			L			0.08	0.04	0.04	0.04	0.04	0.04	0.04	0.00	0.00	33.57	33.2
	5		H	4	4.80		4.84	4.84	4.85	4.85	4.84	4.84	0.00	0.00	7.23	7.5
			L			0.18	0.13	0.13	0.14	0.14	0.13	0.13	0.00	0.00	13.37	12.1

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Tp 100mV [ns]	2	0	HL			60.0	43.6	41.9	51.3	51.3	47.0	46.4	1.2	1.4	3.6	3.2
			LH			60.0	41.8	39.9	47.4	45.7	45.2	43.4	0.8	0.9	6.6	6.0
		2	HL			70.0	42.9	38.7	48.5	44.0	45.9	41.8	0.9	0.8	8.7	11.2
			LH			65.0	42.5	41.5	50.2	49.4	45.9	45.4	1.1	1.2	5.9	5.2
	3.3	0	HL			65.0	43.4	42.4	55.7	54.3	49.1	48.8	1.8	1.7	3.0	3.3
			LH			65.0	41.5	40.6	49.4	46.8	45.8	44.0	1.0	1.0	6.3	7.0
		3.3	HL			75.0	42.1	39.1	50.3	46.4	46.3	43.5	1.2	1.1	7.7	9.2
			LH			70.0	42.4	41.4	52.7	51.0	47.1	46.1	1.5	1.5	5.1	5.2
	5	0	HL			75.0	48.0	47.5	62.8	60.7	54.8	54.1	2.3	2.2	3.0	3.2
			LH			75.0	43.9	42.7	54.3	51.9	49.1	47.7	1.5	1.6	5.8	5.5
		5	HL			85.0	46.7	43.9	58.2	54.6	52.7	50.0	1.9	1.7	5.7	7.0
			LH			75.0	44.3	42.9	59.2	54.1	49.9	48.6	1.8	1.8	4.6	5.0

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Tp 20mV [ns]	2	0	HL			75.0	55.9	56.8	66.4	65.5	60.7	61.1	1.5	1.3	3.2	3.6
			LH			75.0	54.4	53.8	63.7	61.4	59.0	58.1	1.4	1.3	3.9	4.4
		2	HL			100.0	57.7	55.2	64.0	62.2	60.9	59.3	1.1	1.1	12.1	12.5
			LH			105.0	56.8	58.6	84.3	69.4	63.2	63.5	2.0	1.7	7.1	8.2
	3.3	0	HL			80.0	57.2	58.0	69.6	68.4	63.0	63.1	1.8	1.7	3.1	3.3
			LH			85.0	55.9	55.2	67.2	64.6	61.3	60.2	1.6	1.6	5.0	5.2
		3.3	HL			115.0	60.1	56.8	68.4	66.0	64.4	62.0	1.4	1.5	11.9	12.1
			LH			115.0	57.0	58.3	116.8	70.7	64.1	63.9	2.8	2.0	6.1	8.7
	5	0	HL			95.0	61.3	62.0	76.2	74.7	68.5	68.2	2.1	1.9	4.1	4.6
			LH			105.0	59.7	58.8	72.2	70.0	66.1	64.9	1.8	1.8	7.2	7.3
		5	HL			140.0	66.4	62.2	77.8	73.9	72.0	69.0	1.9	1.8	12.0	13.2
			LH			125.0	58.9	59.8	76.5	73.9	67.0	66.4	2.5	2.2	7.8	8.8

% of test with Cpk > 2:	96.5%
% of test with Cpk > 1.67:	100.0%
% of test with Cpk > 1.33:	100.0%

Here are the statistical distributions for each electrical parameter versus datasheet specification.
These results conform to ST mat30 standard results.
All statistical data are showed separately for comp A and comp B in the same package.

[FT -40 °C]

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Vio [mV]	2	-0.2			-10	10	-1.48	-1.41	0.47	0.56	-0.47	-0.35	0.54	0.49	5.90	6.57
		0			-7	7	-1.47	-1.41	0.47	0.57	-0.47	-0.36	0.53	0.49	4.08	4.51
		1					-1.71	-1.10	3.21	3.51	0.26	0.88	1.05	1.05	2.14	1.94
		2					-1.33	-1.15	3.26	3.43	0.41	0.95	0.99	0.95	2.22	2.13
		2.2			-10	10	-1.29	-1.15	3.28	3.43	0.42	0.95	0.99	0.94	3.22	3.20
	3.3	-0.2			-10	10	-1.25	-1.14	1.25	0.77	-0.10	-0.12	0.59	0.48	5.59	6.93
		0			-7	7	-1.25	-1.14	0.73	0.78	-0.23	-0.12	0.53	0.48	4.27	4.83
		1.65					-1.23	-1.14	1.08	0.79	-0.12	-0.12	0.55	0.48	4.18	4.81
		3.3					-1.60	-1.39	3.00	3.07	0.05	0.53	0.97	0.90	2.39	2.39
		3.5			-10	10	-1.61	-1.40	3.04	3.06	0.06	0.53	0.98	0.90	3.40	3.50
	5	-0.2			-10	-10	-4.41	-0.82	5.27	1.06	0.21	0.18	1.51	0.46	2.17	7.08
		0			-7	7	-5.44	-0.83	1.28	1.07	-0.01	0.22	1.13	0.45	2.06	5.07
		2.5					-0.98	-0.83	1.84	1.07	0.17	0.18	0.57	0.47	4.00	4.87
		5					-1.87	-1.58	2.78	2.78	-0.23	0.21	0.97	0.88	2.33	2.56
		5.2			-10	-10	-1.56	-1.58	2.82	2.78	-0.13	0.21	0.91	0.89	3.63	3.68

Cpk < 2: Comparators team agreed with this Cpk to have more competitive Vio limits.

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min	max	avg	stdev	cpk
Icc [uA]	2.0	0.0	H			115.0	76.8	86.5	80.4	1.9	6.0
			L			125.0	88.0	99.4	92.0	2.3	4.8
		2.0	H			150.0	102.8	117.3	107.9	3.0	4.7
			L			130.0	93.2	106.3	97.9	2.6	4.1
	3.3	0.0	H			120.0	78.9	88.6	82.4	2.0	6.4
			L			125.0	90.8	102.2	94.7	2.3	4.5
		3.3	H			155.0	106.3	121.4	111.7	3.1	4.7
			L			140.0	96.0	109.2	100.7	2.7	4.9
	5.0	0.0	H			125.0	81.1	91.1	84.7	2.0	6.8
			L			135.0	94.1	105.7	98.1	2.3	5.3
		5.0	H			160.0	110.2	125.7	115.7	3.2	4.6
			L			140.0	98.9	112.4	103.8	2.8	4.4

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Iib [nA]	2				-300	300	-212.4	-217.0	-176.2	-172.5	-189.9	-188.8	8.7	10.0	4.2	3.7
	3.3						-213.9	-218.7	-177.6	-173.9	-191.4	-190.3	8.7	10.0	4.1	3.7
	5						-215.4	-220.3	-179.0	-175.1	-192.8	-191.7	8.8	10.1	4.1	3.6
Iio [nA]	2				-100	100	0.01	0.85	9.50	9.52	2.31	4.40	1.91	2.55	17.03	12.5
	3.3						0.09	0.70	9.73	9.41	2.36	4.33	1.93	2.52	16.84	12.7
	5						0.12	0.77	9.62	9.39	2.40	4.37	1.93	2.51	16.85	12.7

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
CMRR [dB]	2						56.4	54.7	95.7	104.2	68.6	65.7	9.2	8.8	N/A	N/A
	3.3						62.2	60.7	105.7	91.0	74.8	73.4	8.8	6.8	N/A	N/A
	5						60.7	66.2	101.9	113.2	77.7	81.6	10.0	11.2	N/A	N/A
SVR [dB]							57.5	65.7	77.8	79.1	73.6	74.7	4.1	2.3	N/A	N/A

N/A ... CMRR and SVR in dB have not Normal (Gaussian) distribution

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Voh Vol [V]	2		H	1	1.80		1.93	1.94	1.94	1.94	1.94	1.94	0.00	0.00	8.7	28.2
			L			0.15	0.05	0.05	0.06	0.05	0.05	0.05	0.00	0.00	7.9	26.3
	3.3		H	1	3.10		3.25	3.26	3.26	3.26	3.26	3.26	0.00	0.00	7.0	28.8
			L			0.15	0.03	0.03	0.04	0.04	0.03	0.03	0.00	0.00	8.1	21.9
	5		H	4	4.70		4.84	4.88	4.88	4.88	4.88	4.88	0.01	0.00	N/A	N/A
			L			0.25	0.11	0.11	0.15	0.13	0.12	0.12	0.01	0.00	7.4	21.7

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Tp 100mV [ns]	2	0	HL			80.0	37.1	33.3	42.4	38.1	39.3	35.6	1.2	1.2	11.0	12.5
			LH			80.0	33.4	31.2	37.9	34.9	35.7	32.7	1.1	0.8	13.7	19.0
		2	HL			95.0	35.4	33.7	40.3	39.5	37.9	36.2	1.3	1.1	14.4	18.2
			LH			90.0	38.2	34.4	44.8	43.1	41.0	38.2	1.4	1.9	11.9	8.9
	3.3	0	HL			90.0	38.5	34.2	44.8	39.7	41.2	36.6	1.5	1.4	11.1	12.6
			LH			90.0	33.6	31.6	40.2	37.7	37.5	34.1	1.7	1.4	10.5	13.5
		3.3	HL			100.0	36.9	35.1	42.4	42.7	39.8	38.8	1.4	1.4	14.7	15.0
			LH			95.0	39.2	34.7	47.4	44.2	42.5	39.1	1.7	2.2	10.6	8.4
	5	0	HL			100.0	43.5	38.6	51.7	45.0	46.7	41.6	1.9	1.6	9.4	11.9
			LH			100.0	37.6	34.7	44.2	41.8	41.0	38.0	1.6	1.6	12.3	13.2
		5	HL			115.0	43.9	41.0	51.5	51.5	47.5	45.8	1.9	1.9	11.8	12.3
			LH			100.0	42.0	37.0	51.2	48.0	45.8	41.9	1.9	2.5	9.3	7.7

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Tp 20mV [ns]	2	0	HL			105.0	47.9	45.1	52.5	51.0	49.8	48.3	1.0	1.3	17.9	14.3
			LH			105.0	45.5	44.6	51.5	50.9	48.9	47.5	1.4	1.5	13.3	12.4
		2	HL			140.0	49.9	43.8	55.7	50.9	53.2	47.3	1.3	1.4	21.7	22.3
			LH			145.0	52.9	53.5	62.2	65.2	56.6	58.4	1.7	2.6	17.2	11.2
	3.3	0	HL			110.0	49.6	46.8	55.9	52.9	52.3	50.0	1.4	1.5	13.4	13.1
			LH			120.0	46.4	46.4	53.4	53.3	50.2	49.5	1.6	1.6	14.3	14.7
		3.3	HL			160.0	51.7	46.2	59.4	54.9	56.0	50.3	1.7	1.7	20.9	22.1
			LH			160.0	53.6	53.5	63.9	66.5	57.8	58.9	2.0	2.9	16.7	11.8
	5	0	HL			135.0	53.9	50.9	62.2	58.3	57.4	54.4	1.9	1.9	13.9	14.4
			LH			145.0	49.5	49.7	57.8	57.9	53.8	53.4	2.0	2.0	15.2	15.5
		5	HL			195.0	57.6	52.2	66.3	62.7	62.2	57.1	1.9	2.0	23.3	22.6
			LH			175.0	55.2	54.6	66.7	69.2	60.1	60.7	2.3	3.1	16.4	12.2

% of test with Cpk > 2:	98.4%
% of test with Cpk > 1.67:	100.0%
% of test with Cpk > 1.33:	100.0%

Here are the statistical distributions for each electrical parameter versus datasheet specification.
These results conform to ST mat30 standard results.
All statistical data are showed separately for comp A and comp B in the same package.

[FT 125 °C]

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
		-0.2			-10	10	-2.52	-2.70	3.15	3.42	-0.27	-0.35	1.24	1.16	2.61	2.76
		0					-2.68	-1.90	0.62	0.66	-0.67	-0.47	0.74	0.69	2.85	3.17
	2	1			-7	7	-1.87	-1.88	0.66	0.69	-0.59	-0.45	0.65	0.69	3.27	3.17
		2					-1.21	-1.18	2.80	3.39	0.52	0.82	0.86	0.95	2.50	2.16
		2.2			-10	10	-1.23	-1.17	2.82	2.84	0.52	0.77	0.86	0.91	3.66	3.40
		-0.2			-10	10	-2.61	-2.47	2.49	2.50	-0.09	0.06	1.34	1.29	2.46	2.57
		0					-1.79	-1.44	1.03	1.06	-0.28	-0.07	0.72	0.68	3.12	3.41
Vio [mV]	3.3	1.65			-7	7	-1.76	-1.43	1.02	1.05	-0.28	-0.07	0.71	0.67	3.16	3.45
		3.3					-1.77	-1.52	2.46	2.35	0.01	0.23	0.85	0.87	2.74	2.60
		3.5			-10	10	-1.78	-1.51	2.47	2.34	0.02	0.23	0.85	0.87	3.92	3.76
		-0.2			-10	-10	-1.70	-2.32	3.85	3.78	0.77	0.92	1.45	1.58	2.12	1.91
		0					-1.84	-0.87	1.56	1.57	0.19	0.44	0.77	0.67	2.96	3.27
	5	2.5			-7	7	-1.84	-0.89	1.56	1.55	0.18	0.41	0.76	0.67	2.97	3.27
		5					-1.82	-1.81	2.14	1.96	-0.38	-0.20	0.81	0.85	2.74	2.66
		5.2			-10	-10	-1.82	-1.81	2.14	1.96	-0.37	-0.20	0.81	0.85	3.98	3.83

Cpk < 2: Comparators team agreed with this Cpk to have more competitive Vio limits.

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min	max	avg	stdev	cpk
		0.0	H			115.0	61.2	65.6	62.6	1.0	14.6
	2.0		L			125.0	70.7	76.0	72.4	1.1	15.4
		2.0	H			150.0	86.3	94.1	88.7	1.7	12.2
			L			130.0	76.8	83.9	79.0	1.5	11.7
		0.0	H			120.0	62.9	67.3	64.2	1.0	15.1
Icc [uA]	3.3		L			125.0	72.7	78.1	74.5	1.1	14.6
		3.3	H			155.0	88.9	96.9	91.4	1.8	12.0
			L			140.0	79.1	86.0	81.1	1.5	13.1
		0.0	H			125.0	64.8	69.5	66.2	1.0	15.2
	5.0		L			135.0	75.3	80.9	77.3	1.2	16.1
		5.0	H			160.0	91.7	100.5	94.4	1.9	11.6
			L			140.0	81.4	88.7	83.5	1.6	11.9

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Iib [nA]	2						-58.0	-59.7	-50.0	-50.4	-52.4	-52.8	1.8	1.8	45.7	45.1
	3.3				-300	300	-58.1	-59.8	-50.2	-50.6	-52.6	-53.0	1.8	1.8	45.6	45.1
	5						-58.4	-60.1	-50.3	-50.7	-52.7	-53.2	1.8	1.9	45.1	44.3
Iio [nA]	2						0.14	1.60	1.33	2.79	0.67	2.11	0.24	0.26	139.86	124.1
	3.3				-100	100	0.04	1.52	1.32	3.00	0.65	2.16	0.27	0.28	120.86	118.4
	5						0.12	1.70	1.20	2.98	0.57	2.26	0.28	0.31	118.83	104.2

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
CMRR [dB]	2						54.9	54.9	101.1	88.0	67.2	65.7	10.6	8.3	N/A	N/A
	3.3						61.8	61.9	113.9	98.7	75.9	73.7	11.2	7.4	N/A	N/A
	5						65.1	63.7	110.5	101.4	78.2	77.4	9.6	8.6	N/A	N/A
SVR [dB]							68.6	62.7	77.5	72.8	70.8	70.5	1.2	1.4	N/A	N/A

N/A ... CMRR and SVR in dB have not Normal (Gaussian) distribution

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Voh Vol [V]	2		H	1	1.80		1.90	1.90	1.90	1.90	1.90	1.90	0.00	0.00	28.8	28.0
			L			0.15	0.09	0.09	0.09	0.09	0.09	0.09	0.00	0.00	25.1	25.0
	3.3		H	1	3.10		3.24	3.24	3.24	3.24	3.24	3.24	0.00	0.00	30.0	29.2
			L			0.15	0.06	0.06	0.06	0.06	0.06	0.06	0.00	0.00	33.6	33.3
	5		H	4	4.70		4.80	4.80	4.81	4.81	4.81	4.81	0.00	0.00	17.4	17.3
			L			0.25	0.19	0.19	0.20	0.19	0.19	0.19	0.00	0.00	10.7	10.8

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Tp 100mV [ns]	2	0	HL			80.0	56.8	55.1	61.3	59.4	59.1	57.4	1.0	1.0	7.0	7.6
			LH			80.0	53.5	51.8	58.2	56.2	56.4	54.0	1.0	0.9	7.6	9.1
		2	HL			95.0	52.6	48.9	56.3	52.2	54.5	51.3	0.8	0.6	16.9	23.5
			LH			90.0	53.3	52.0	57.2	57.0	55.0	54.7	0.9	1.2	12.5	10.1
	3.3	0	HL			90.0	59.6	57.4	65.7	63.2	62.9	60.3	1.3	1.3	6.8	7.5
			LH			90.0	54.7	52.7	61.0	58.6	58.5	55.5	1.4	1.3	7.7	8.9
		3.3	HL			100.0	53.6	49.4	59.0	54.6	56.3	53.1	1.1	1.0	13.0	16.0
			LH			95.0	54.1	51.4	59.8	57.5	56.7	54.7	1.3	1.6	10.2	8.5
	5	0	HL			100.0	65.2	63.0	72.4	69.7	69.1	66.1	1.6	1.6	6.4	7.1
			LH			100.0	58.1	56.2	66.2	63.9	63.0	59.7	1.7	1.7	7.3	8.0
		5	HL			115.0	59.5	55.0	67.0	62.2	63.3	60.0	1.5	1.4	11.8	13.1
			LH			100.0	56.9	53.0	63.9	60.9	60.0	57.3	1.5	2.0	8.7	7.2

Para-meter	Vcc [V]	Vcm [V]	Out [H/L]	Iout [mA]	min limit	max limit	min A	min B	max A	max B	avg A	avg B	stdev A	stdev B	cpk A	cpk B
Tp 20mV [ns]	2	0	HL			105.0	73.5	73.9	80.7	80.1	77.2	77.2	1.6	1.5	5.8	6.2
			LH			105.0	74.2	74.1	82.3	81.0	79.0	77.4	1.7	1.5	5.0	6.1
		2	HL			140.0	67.8	65.3	74.0	71.6	71.3	69.7	1.3	1.2	17.8	19.7
			LH			145.0	75.1	74.3	82.3	82.5	78.5	78.3	1.6	1.9	13.8	11.5
	3.3	0	HL			110.0	76.4	76.2	85.1	83.5	80.8	79.8	1.9	1.8	5.0	5.7
			LH			120.0	76.1	76.4	86.1	84.8	82.0	80.3	2.1	1.9	6.0	6.9
		3.3	HL			160.0	69.9	66.7	77.7	74.6	74.2	72.0	1.6	1.5	18.3	20.2
			LH			160.0	74.6	73.4	83.4	82.9	78.7	78.1	1.9	2.3	14.1	12.1
	5	0	HL			135.0	82.7	82.2	93.1	91.2	88.1	86.4	2.3	2.1	6.9	7.6
			LH			145.0	81.1	81.3	92.6	91.5	87.8	86.1	2.5	2.3	7.7	8.4
		5	HL			195.0	76.6	72.6	87.4	83.1	82.4	79.4	2.0	1.9	18.5	20.4
			LH			175.0	76.6	75.1	86.8	86.2	81.6	80.6	2.2	2.7	14.0	11.8

% of test with Cpk > 2:	98.4%
% of test with Cpk > 1.67:	100.0%
% of test with Cpk > 1.33:	100.0%

3.2. Certificate of ESD

CERTIFICATE OF ELECTROSTATIC DISCHARGE SENSITIVITY

ACCORDING TO THE PROCEDURE N°0060102

and is compliant with the following standards :

- **MIL883C**
- **JEDEC JESD22**
- **ANSI ESD STM 5.1**

Operator's name: Karel Znojemský (HBM, MM), Luca Cantarella (CDM)
Date: 4 May 2009 (HBM, MM), 28 April 2009 (CDM)
Commercial product: TS3022ID (SO8), TS3022IST (miniSO8)
Die code: F3022CCL
Package: SO8, miniSO8
Traceability code: CZ912083 (SO8), 9Y907679 (miniSO8)

☒ **HBM (Human Body Model)**

Equipment reference: KeyTek ZapMaster MK.2 SE1, S/N 0407277
Number of units: 3 (SO8) + 3 (miniSO8)
This product meets the electrostatic discharge resistance specification of 5kV

☒ **MM (Machine Model)**

Equipment reference: KeyTek ZapMaster MK.2 SE1, S/N 0407277
Number of units: 3 (SO8) + 3 (miniSO8)
This product meets the electrostatic discharge resistance specification of 300V

☒ **CDM (Charged Device Model)**

Equipment reference: Orion CDM Test System S/N 20023
Number of units: 5 (SO8) + 5 (miniSO8)
This product meets the electrostatic discharge resistance specification of 1.5kV

3.3. Certificate of Latch-up

CERTIFICATE OF LATCH-UP

ACCORDING TO THE PROCEDURE N°0018695

Operator's name: Karel Znojemský
Date: 4 May 2009
Die code: F3022CCL
Package: SO8
Traceability code: CZ912083 (SO8)
LATCH-UP tester reference: KeyTek ZapMaster MK.2 SE1, S/N: 0407277

CURRENT INJECTION			Injection **+**		**Class**	Injection **-**		**Class**
	Pin n°	Type	I (mA)	V(V)		-I (mA)	-V (V)	
INPUTS	2, 6	Invert	200	6.3	**A**	200	-1.1	**A**
	3, 5	Non Invert	200	6.3	**A**	200	-1.1	**A**
OUTPUTS	1, 7	Low output	200	6.2	**A**	200	-1.1	**A**
		High output	200	6.2	**A**	200	-1.1	**A**

SUPPLY VOLTAGE	Latch-up	No Latch-up
Overvoltage		**OK (Class A)**
Supply cut		**OK**

Test type	**Trigger polarity**	**Quality Level**	**Trigger stress**
Supply voltage		**A**	2xVmax or 500mA
		B	1.5xVmax or 1.5xInom or Inom+100mA
Current injection	Positive	**A**	2xVmax or 200mA
		B	1.5xVmax or 1.5xInom or Inom+100mA
	Negative	**A**	-2xVmax or -200mA
		B	-1.5xVmax or -0.5xInom or -100mA
		C	If limit of level B is not achieved

Note:
All device parameters were measured before and after test, no changes occurred.

4. Cp, Cpk explanation

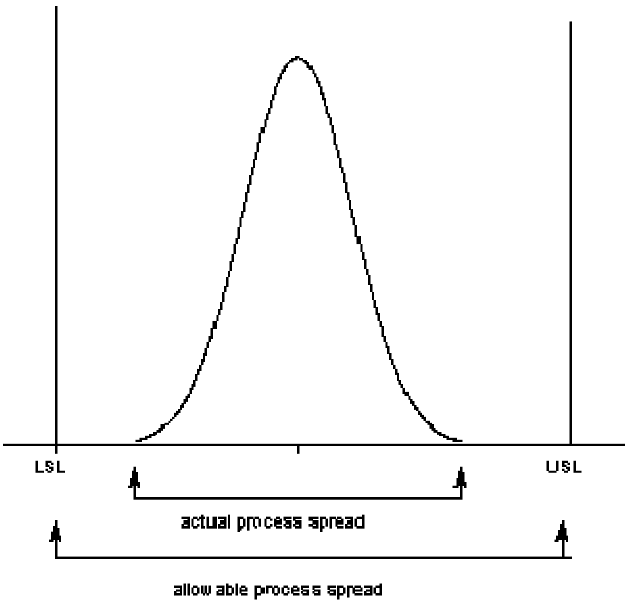
What is Process Capability?

Process capability compares the output of an *in-control* process to the specification limits by using *capability indices*. The comparison is made by forming the ratio of the spread between the process specifications (the specification "width") to the spread of the process values, as measured by 6 process standard deviation units (the process "width").

Process Capability Indices

We are often required to compare the output of a stable process with the process specifications and make a statement about how well the process meets specification. To do this we compare the natural variability of a stable process with the process specification limits.

A capable process is one where almost all the measurements fall inside the specification limits. This can be represented pictorially by the plot below:



There are several statistics that can be used to measure the capability of a process: C_p, C_{pk}, C_{pm}.

Most capability indices estimates are valid only if the sample size used is 'large enough'. Large enough is generally thought to be about 50 independent data values.

The C_p, C_{pk}, and C_{pm} statistics assume that the population of data values is normally distributed. Assuming a two-sided specification, if μ and σ are the mean and standard deviation, respectively, of the normal data and USL, LSL, and T are the upper and lower specification limits and the target value, respectively, then the population capability indices are defined as follows:

$$C_p = \frac{USL - LSL}{6\sigma}$$

$$C_{pk} = \min\left[\frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma}\right]$$

$$C_{pm} = \frac{USL - LSL}{6\sqrt{\sigma^2 + (\mu - T)^2}}$$

Sample estimators for these indices are given below. (Estimators are indicated with a "hat" over them).

$$\hat{C}_p = \frac{USL - LSL}{6s}$$

$$\hat{C}_{pk} = \min \left[\frac{USL - \bar{x}}{3s}, \frac{\bar{x} - LSL}{3s}\right]$$

$$\hat{C}_{pm} = \frac{USL - LSL}{6\sqrt{s^2 + (\bar{x} - T)^2}}$$

The estimator for C_{pk} can also be expressed as $C_{pk} = C_p(1-k)$, where k is a scaled distance between the midpoint of the specification range, m, and the process mean, μ.

Denote the midpoint of the specification range by m = (USL+LSL)/2. The distance between the process mean, μ, and the optimum, which is m, is μ- m, where $m \leq \mu \leq LSL$. The scaled distance is

$$k = \frac{|m - \mu|}{(USL - LSL)/2}, \qquad 0 \leq k \leq 1$$

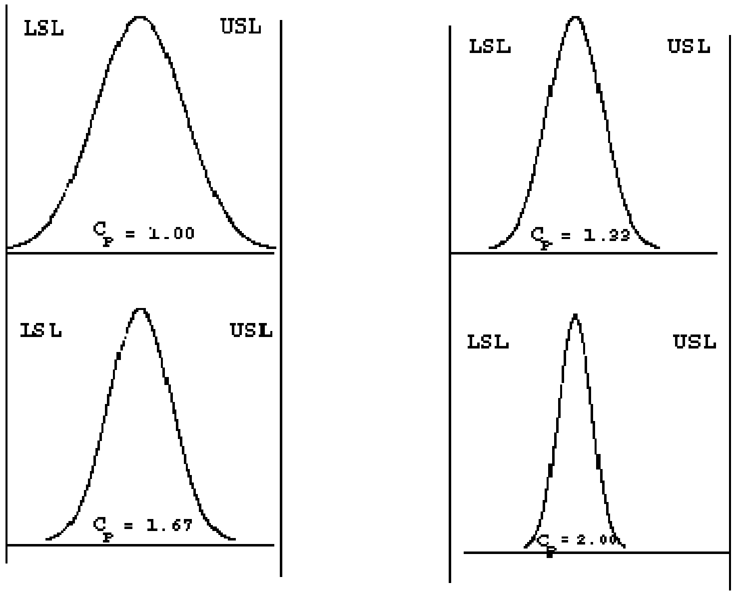
(the absolute sign takes care of the case when $LSL \leq \mu \leq m$). To determine the estimated value, $\hat{k}$, we estimate μ by $\bar{x}$. Note that $\bar{x} \leq USL$.

The estimator for the C_p index, adjusted by the k factor, is

$$\hat{C}_{pk} = \hat{C}_p(1 - \hat{k})$$

Since $0 \leq k \leq 1$, it follows that $\hat{C}_{pk} \leq \hat{C}_p$.

To get an idea of the value of the C_p statistic for varying process widths, consider the following plot



This can be expressed numerically by the table below:

USL - LSL	6σ	8σ	10σ	12σ
C_p	1.00	1.33	1.66	2.00
Rejects	.27%	64 ppm	.6 ppm	2 ppb
% of spec used	100	75	60	50

where ppm = parts per million and ppb = parts per billion. Note that the reject figures are based on the assumption that the distribution is centered at μ.

We have discussed the situation with two spec. limits, the USL and LSL. This is known as the *bilateral* or two-sided case. There are many cases where only the lower or upper specifications are used. Using one spec limit is called *unilateral* or one-sided. The corresponding capability indices are

$$C_{pu} = \frac{\text{allowable upper spread}}{\text{actual upper spread}} = \frac{USL - \mu}{3\sigma}$$

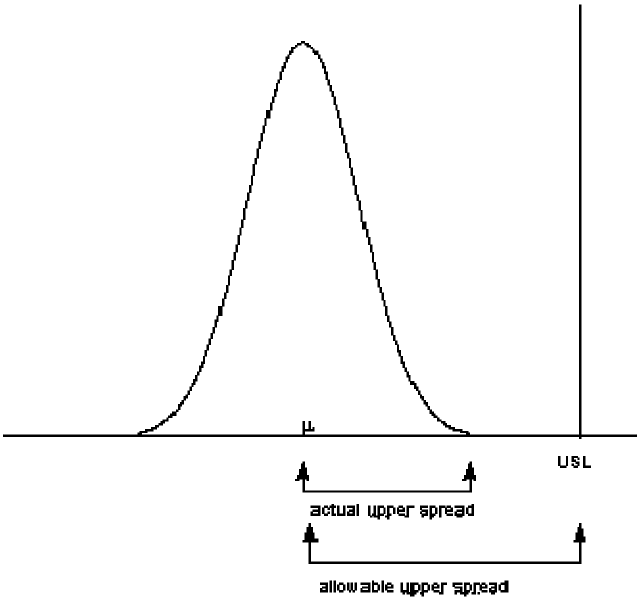
and

$$C_{pl} = \frac{\text{allowable lower spread}}{\text{actual lower spread}} = \frac{\mu - LSL}{3\sigma}$$

where μ and σ are the process mean and standard deviation, respectively.

Estimators of C_{pu} and C_{pl} are obtained by replacing μ and σ by $\bar{x}$ and s, respectively. The following relationship holds

$C_p = (C_{pu} + C_{pl}) /2$.
This can be represented pictorially by



Note that we also can write:

C_{pk} = min {C_{pl}, C_{pu}}.

Confidence Limits For Capability Indices

Assuming normally distributed process data, the distribution of the sample $\hat{C}_p$ follows from a Chi-square distribution and $\hat{C}_{pu}$ and $\hat{C}_{pl}$ have distributions related to the non-central *t* distribution. Fortunately, approximate confidence limits related to the normal distribution have been derived. Various approximations to the distribution of $\hat{C}_{pk}$ have been proposed, including those given by Bissell (1990), and we will use a normal approximation.

The resulting formulas for confidence limits are given below:

100(1-α)% Confidence Limits for C_p

$$Pr\{\hat{C}_p(L_1) \leq C_p \leq \hat{C}_p(L_2)\} = 1 - \alpha$$

where

$$L_1 = \sqrt{\frac{\chi^2_{(\nu,\alpha/2)}}{\nu}} \qquad L_2 = \sqrt{\frac{\chi^2_{(\nu,1-\alpha/2)}}{\nu}}$$

ν= degrees of freedom

Approximate 100(1-α)% confidence limits for C_{pu} with sample size *n* are:

$$C_{pu}(lower) = \hat{C}_{pu} - z_{1-\beta}\sqrt{\frac{1}{9n} + \frac{\hat{C}^2_{pu}}{2(n-1)}}$$

$$C_{pu}(upper) = \hat{C}_{pu} + z_{1-\alpha}\sqrt{\frac{1}{9n} + \frac{\hat{C}_{pu}^2}{2(n-1)}}$$

with *z* denoting the percent point function of the standard normal distribution. If β is not known, set it to α.

Limits for C_{pl} are obtained by replacing $\hat{C}_{pu}$ by $\hat{C}_{pl}$.

Zhang et al. (1990) derived the exact variance for the estimator of C_{pk} as well as an approximation for large *n*. The reference paper is Zhang, Stenback and Wardrop (1990), "Interval Estimation of the process capability index", *Communications in Statistics: Theory and Methods*, 19(21), 4455-4470.

The variance is obtained as follows:

Let

$$c = \sqrt{n}[\mu - (USL + LSL)/2]\sigma$$

$$d = (USL - LSL)/\sigma$$

$$\Phi(-c) = \int_{-inf}^{-c} \frac{1}{\sqrt{2\pi}} \exp -5z^2 dz$$

Then

$$Var(\hat{C}_{pk})$$

$$= (d^2/36)(n-1)(n-3)$$

$$-(d/9\sqrt{n})(n-1)(n-3)\{\sqrt{2\pi}\exp(-c^2/2) + c[1-2\Phi(-c)]\}$$

$$+[(1/9)(n-1)/(n(n-3))](1+c^2)$$

$$-[(n-1)/(72n)]\{\frac{\Gamma((n-2)/2)}{\Gamma((n-1)/2)}\}^2$$

$$*\{d\sqrt{n} - 2\sqrt{2\pi}\exp(-c^2/2) - 2c[1-2\Phi(-c)]\}^2$$

Their approximation is given by:

$$Var(\hat{C}_{pk}) = \frac{n-1}{n-3} - 0.5\{\frac{\Gamma((n-2)/2)}{\Gamma((n-1)/2)}\}^2$$

where

$$n \geq 25, 0.75 \leq C_{pk} \leq 4, \quad |c| \leq 100, \text{ and } \quad d \leq 24$$

The following approximation is commonly used in practice

$$C_{pk} = \hat{C}_{pk} \pm z_{1-\alpha/2}\sqrt{\frac{1}{9n} + \frac{\hat{C}_{pk}^2}{2(n-1)}}$$

It is important to note that the sample size should be at least 25 before these approximations are valid. In general, however, we need $n \geq 100$ for capability studies. Another point to observe is that variations are not negligible due to the randomness of capability indices.

Capability Index Example

For a certain process the USL = 20 and the LSL = 8. The observed process average, $\bar{X}$= 16, and the standard deviation, *s* = 2. From this we obtain

$$\hat{C}_p = \frac{USL - LSL}{6s} = \frac{20-8}{6(2)} = 1.0$$

This means that the process is capable as long as it is located at the midpoint, m = (USL + LSL)/2 = 14.

But it doesn't, since $\bar{x}$= 16. The $\hat{k}$ factor is found by

$$\hat{k} = \frac{|m - \bar{x}|}{(USL - LSL)/2} = \frac{2}{6} = 0.3333$$

and

$$\hat{C}_{pk} = \hat{C}_p(1 - \hat{k}) = 0.6667$$

We would like to have $\hat{C}_{pk}$ at least 1.0, so this is not a good process. If possible, reduce the variability or/and center the process. We can compute the $\hat{C}_{pu}$ and $\hat{C}_{pl}$

$$\hat{C}_{pu} = \frac{USL - \bar{x}}{3s} = \frac{20-16}{3(2)} = 0.6667$$

$$\hat{C}_{pl} = \frac{\bar{x} - LSL}{3s} = \frac{16-8}{3(2)} = 1.3333$$

From this we see that the $\hat{C}_{pu}$, which is the smallest of the above indices, is 0.6667. Note that the formula $\hat{C}_{pk} = \hat{C}_p(1 - \hat{k})$ is the algebraic equivalent of the *min*{ $\hat{C}_{pu}$, $\hat{C}_{pl}$ } definition.

What happens if the process is not approximately normally distributed?

The indices that we considered thus far are based on normality of the process distribution. This poses a problem when the process distribution is not normal. Without going into the specifics, we can list some remedies.

1. Transform the data so that they become approximately normal. A popular transformation is the Box-Cox transformation
2. Use or develop another set of indices, that apply to nonnormal distributions. One statistic is called C_{npk} (for non-parametric C_{pk}). Its estimator is calculated by

$$\hat{C}_{npk} = \min\left[\frac{USL - median}{p(.995) - median}, \frac{median - LSL}{median - p(.005)}\right]$$

where *p*(0.995) is the 99.5th percentile of the data and *p*(.005) is the 0.5th percentile of the data.

For additional information on nonnormal distributions, see Johnson and Kotz (1993).

There is, of course, much more that can be said about the case of nonnormal data. However, if a Box-Cox transformation can be successfully performed, one is encouraged to use it.

Source:
The National Institute of Standards and Technology
NIST is an agency of the U.S. Commerce Department's Technology Administration.

5. Product Design Qualification & Production FC

PRODUCT DESIGN QUALIFICATION FLOW

"Quality is what the customer says it is."
Tom Peters

Manufacturing and reliability must be considered at the design level in order to manufacture reliable products meeting customers' expectations.

New product development plans adopt the Quality Function Deployment **(QFD)** methodology as a basic tool to understand customers' requirements. This formally translates the customers' need into technical requirements as product specifications, process operations and manufacturing process controls, that represent the key points for the product finalization.

In SGS-THOMSON, a corporate procedure defines the product maturity, specifying three maturity levels with rules from one level to the next. They are: design, engineering and production. In addition there are various sub levels. This procedure governs the entire life cycle of a product from new product proposal to its obsolescence. It also determines when and how, engineering samples can be released at sub-maturity levels in a controlled manner by defining "for application study only" or "not yet fully qualified" on the customer documentation.

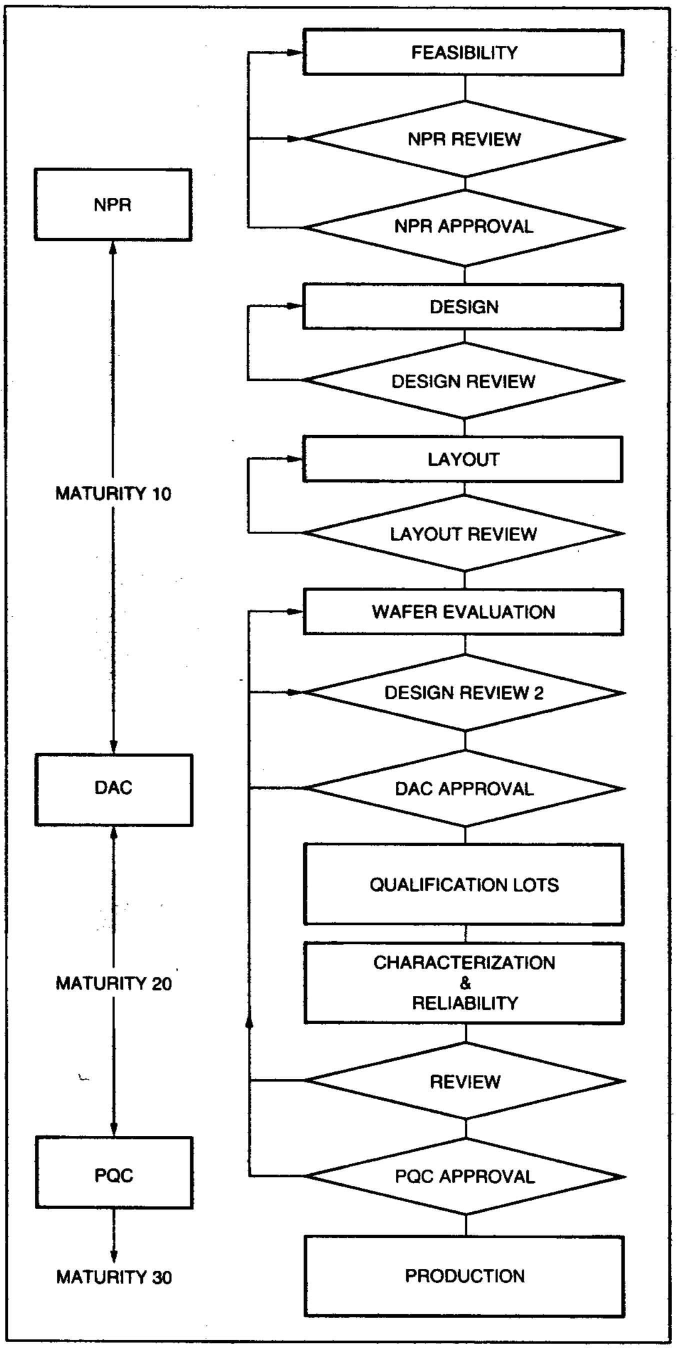
Each new product begins from the preparation of a target specification and a document called a New Product Request **(NPR)**, which contains business and technical details. The purpose of this first control is to evaluate the potential of the product and determine if there is sufficient justification to allocate design resources.

Once the NPR is approved the designers can start work. Designers work to clearly defined design rules which incorporate robust design principles. When the design is complete and the first working samples are available they are evaluated to make sure that the design is acceptable for the next phase, Engineering.

The results of these tests are included in the next key document, the Design Approval Certificate **(DAC)**. The approval of the DAC commits the company to a major investment so it is essential to ensure that the product is ready to proceed.

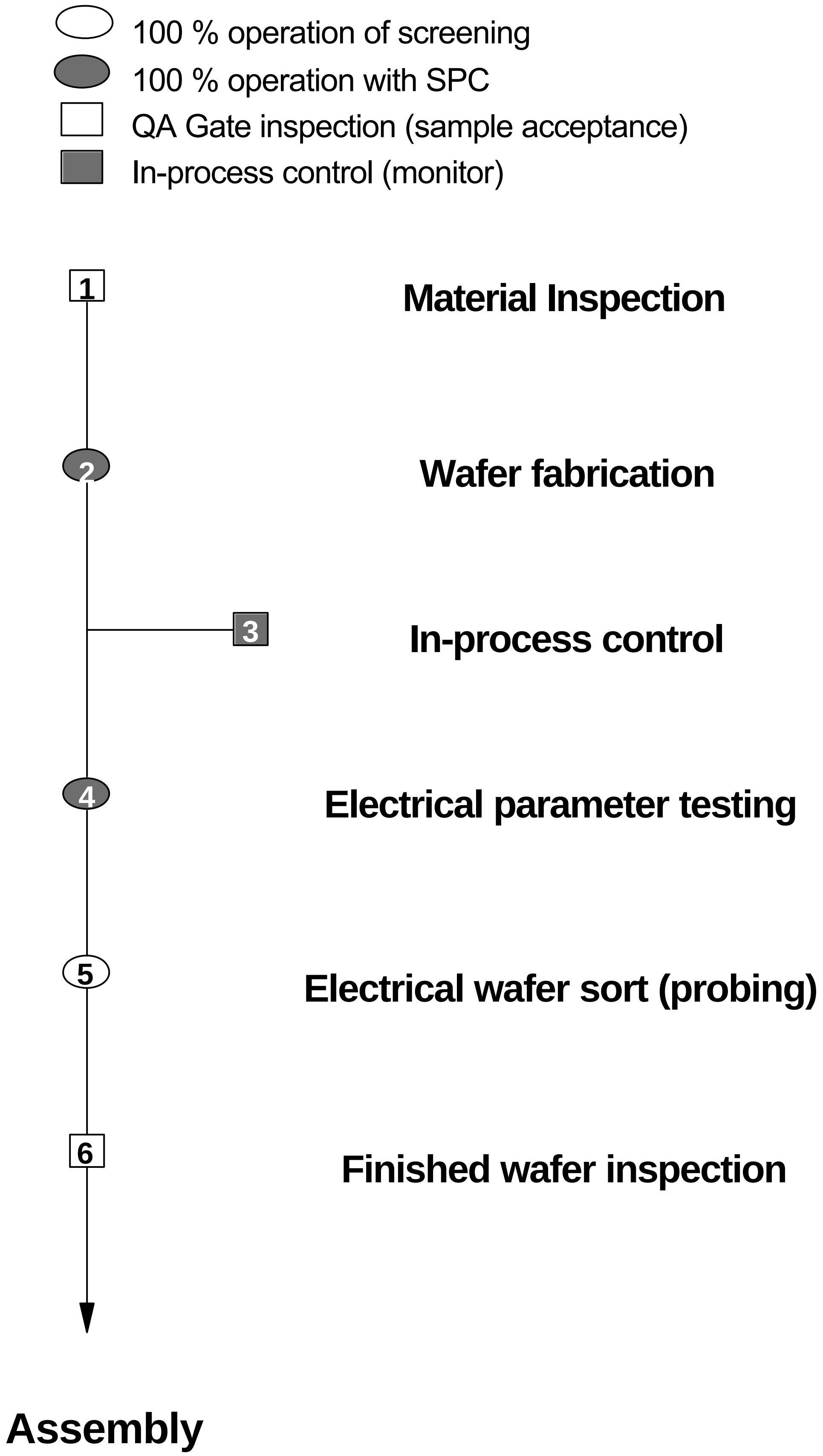
While a product is in design and characterization (maturity 10 & 20), samples may be given to customers with the documentation indicating "engineering samples for application study only and at the customers' risk" under the responsibility of the Division Manager.

New product is prepared for qualification through product characterization and reliability testing. A Product Qualification Certificate **(PQC)** which permits the new product to proceed to manufacturing must be approved by Group Management.



Product design qualification flow

WAFER FAB TYPICAL PRODUCTION PROCESS FLOW CHART



ASSEMBLY TYPICAL PRODUCTION PROCESS FLOW CHART

- (oval) 100 % operation of screening
- (open box) QA Gate inspection (sample acceptance)
- (filled box) In-process control (monitor)