PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MIC/09/4944
Notification Date 09/18/2009

Qualification of ST Muar (Malaysia) TQFP 10x10 assembly line in preplated frame (PPF) and phase out of ST Malta TQFP 10x10 assembly line

Table 1. Change Implementation Schedule

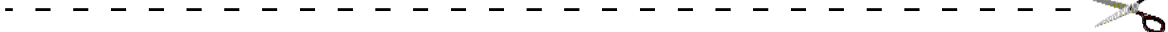
Forecasted implementation date for change	11-Dec-2009
Forecasted availabillity date of samples for customer	16-Nov-2009
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	16-Nov-2009
Estimated date of changed product first shipment	11-Dec-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	All MCUs in TQFP 10x10 44 & 64 pins
Type of change	Package assembly material change
Reason for change	Phase out of ST Malta TQFP 10x10 assembly line
Description of the change	Following PCN MMS-MIC/08/4102 dated 10/20/2008 announcing the qualification of ST Muar for our devices in TQFP 10x10 in pure tin, the Microcontroller division is pleased to announce the qualification of the same assembly line in preplated frame (PPF), ie lead termination in Ni Pd Au. This lead termination is identical to the one used in ST Malta for all MCUs in this package. Thanks to this new qualification, all TQFP 10x10 MCUs currently produced in ST Malta will be transferred to ST Muar according to the timing defined above. Production in ST Malta will be totally phased out by end of this year. There are no changes to the design or external part number as a result of this change. Details of the production for each of the involved product families are given page 5.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Marking from "e3" to "e4"
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MIC/09/4944**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 09/18/2009**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Colonna, Daniel	Division Marketing Manager
Nicholas, Jimmy Edward	Division Product Manager
Narche, Pascal	Division Q.A. Manager

Details of the PCN MMS-MIC/09/4944 are as follow:

Terms and conditions

Customer notification on: 11th-Sep-09

Estimated date of changed product first shipment: 11th-Dec-2009

Manufacturing strategy

	ST Malta	ST Muar (PCN4102)	ST Muar (PCN4944)
ST7	PPF	Pure tin done	PPF
STM32	PPF	None [1]	PPF
STM8	PPF	None [1]	PPF
STR7	PPF	None [1]	PPF

[1] : Manufacturing in Muar delayed in order to ramp up directly in PPF.

For more information, please contact your local Sales & Marketing.

MCD Pkg09 09 QUALIFICATION PLAN

Qualification of : LQFP10*10/ PPF frame at ST Muar

Qualification Reference :	**MCD Pkg09 09**
Issued on :	**Sept 7, 2008**
Assembly Plant :	**ST Muar**
Assembly Line :	**QFP**
Package / Process :	**LQFP 10*10/ PPF**
Lead termination:	**Ni-Pd-Au**

Test Vehicles :

RL Code	**Package**	**Number of Lots**
U75W*412XXXA	LQFP64	3 for qualification
*X25W*405XXXY*	*LQFP64*	*1 for monitoring only*
*XE4Y*854XXX3*	*LQFP44*	*1 for monitoring only*
*U24Y*765ZZZX*	*LQFP44*	*1 for monitoring only*

Test Vehicle Features:

Die information

Test Vehicle	**STM32F101R6T6A**	*STR755FR2T6*
Rawline	**U75W*412XXXA**	*X25W*405XXXY*
psfdescr	**F412XXXA**	*F405XXXY*
Wafer Fab	**TSF3**	*ST Rousset 8”*
FAB Process	**0.18 Gen.Emb.Flash logic**	*CMOSM8T*
Die BackSide	**Lapped silicon**	*Lapped Silicon*
Passivation	**HDPox 10kA+ SRO 1.5kA + PESIN 6kA**	*SiN (nitride)*
Die Step X	**2970 µm**	*4228µm*
Die Step Y	**2970 µm**	*5344µm*
Die Thickness	**381+/-25 µm**	*375+/-25µm*
Pad Open X	**65µm**	*65µm*
Pad Open Y	**70 µm**	*70 µm*
Min Pad Pitch	**80 µm**	*92.8µm*

Test Vehicle	*ST72F324BJ6T6*	*STM8S207S6T6C*
Rawline	*XE4Y*854XXX3*	*U24Y*765ZZZX*
psfdescr	*F854XXX3*	*F765XXXX*
Wafer Fab	*ST Catania 8”*	*ST Rousset 8”*
FAB Process	*CMOSM6DT*	*CMOSF9 0.13µm*
Die BackSide	*Lapped Silicon*	*Lapped Silicon*
Passivation	*USG + PSG + SiOn*	*USG + NitUV (HFP USG+UV Nitride)*
Die Step X	*3050 µm*	*3010 µm*
Die Step Y	*3980 µm*	*2458 µm*
Die Thickness	*375+/-25µm*	*375+/-25µm*
Pad Open X	*100 µm*	*80 µm*
Pad Open Y	*100 µm*	*80 µm*
Min Pad Pitch	*150 µM*	*80.36 µm*

Assembly information

Test Vehicle	**STM32F101R6T6A**	*STR755FR2T6*
Rawline	**U75W*412XXXA**	*X25W*405XXXY*
Assembly Plant	**ST MUAR**	
Packaging	**5W LQFP 64 10x10x1.4**	
POA	**0051434**	
BSA	**CD00240916**	*CD00240624*
B/D	**8197982 REV A**	*7887559 REV C*
	MBD FOR : 5W*412 CUT1	*M&BD FOR: 5W*405 CAN*
	MUAR	*MALTA /MUAR*
Materials	**FRAME TQFP 64L 10x10 6x6mm PPF**	
	GLUE HITACHI EN4900	
	RESIN SUMITOMO EME-G700F	
	WIRE Au D1	
Ecopack	**G (Ecopack2)**	
E Mark	**e4**	
2nd Level Interco	**Precious metal (Ag, Au, NiPdAu)**	
MSL	**3**	
Peak Body Temp (C)	**260°C**	

Test Vehicle	*ST72F324BJ6T6*	*STM8S207S6T6C*
Rawline	*XE4Y*854XXX3*	*U24Y*765ZZZX*
Assembly Plant	*ST MUAR*	
Packaging	*4Y LQFP 44 10x10x1.4*	
POA	*0076922*	
BSA	*CD00246630*	*CD00228927*
B/D	*7607586 REV B*	*8089418 REV C*
	*M&BD FOR : 4Y*854 CUT1*	*MBD FOR : 4Y*765 CUT2*
	MALTA/MUAR	*MALTA / MUAR*
Materials	*FRAME TQFP 44L 10x10 6x6mm PPF*	
	GLUE HITACHI EN4900	
	RESIN SUMITOMO EME-G700F	
	WIRE Au D 0.8	
Ecopack	*G (Ecopack2)*	
E Mark	*e4*	
2nd Level Interco	*Precious metal (Ag, Au, NiPdAu)*	
MSL	*3*	
Peak Body Temp (C)	*260°C*	

Package Reliability Trials :

Reliability Trial		Test Conditions	Pass Criteria	Unit per Lot
Preconditioning JL3+ AC	JL3+ Pressure Pot	121°C, 100% RH, 2 Atm	240h	80
Preconditioning JL3+ HTSL	JL3+ High Temperature Storage	150°C, Unbiased	500h,1000h	80
Preconditioning JL3+ TC	JL3+ Thermal Cycling MIL Std 883, Method 1010	-40°C, +150°C	500Cy,1000Cy	80
Preconditioning JL3+ THS	JL3+ Temperature Humidity Storage	85°C, 85% RH,Unbiased	500h,1000h	80

Package oriented tests/ Trials description

1. **Preconditioning**

According to ST spec 0098044.
Preconditioning test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good modelization of the life of the packaged product.
Out-of-bag floor life storage and soldering are modeled by the following test sequence:

- Bake to completely remove moisture from the package;
- Moisture soak according to the package moisture level;
- IR reflow.

The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder report process. This phenomenon can create plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.

2. **Autoclave (AC)**

The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.

Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
To point out critical water entry paths with consequent electrochemical and galvanic corrosion.

3. Temperature Cycling (TC)

The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).

Purpose: to investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system.

Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.

4. Temperature Humidity Storage (THS)

The Temperature Humidity Storage is stored at controlled conditions of high temperature and relative humidity.

The Temperature Humidity Storage follows the same method than Unbiased HAST at lower temperature.

Purpose: to evaluate the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.
Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package.

- Test conditions: 85°C / 85% RH.
- No power supply

5. High Temperature Storage Life (HTSL)

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.

Purpose: to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.

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