

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-DIS/09/4781 Notification Date 08/19/2009

APM - ASD & IPAD Division Protection Devices in SMA/B/C & STmite Conversion to ECOPACK(r)2 grade - Die design optimisation of Transils in SMA/B<100V

Table 1.	Change	Implementation	Schedule
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Forecasted implementation date for change	28-Aug-2009
Forecasted availabillity date of samples for customer	12-Aug-2009
Forecasted date for STMicroelectronics change Qualification Plan results availability	12-Aug-2009
Estimated date of changed product first shipment	19-Nov-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	Protection Devices in SMA/B/C & STmite packages
Type of change	Multiple types of changes
Reason for change	To meet environmental and technical requirements of the market
Description of the change	The ECOPACK(r) program is the cornerstone of our efforts for being leader in offering environmentally friendly packaging. Progressing in this program, ST is implementing technical solutions designed to progressively remove banned substances from manufacturing. To meet the so called "Halogen-Free" requirements of the market, ST is converting its Protection Devices in SMA/B/C and STmite packages to the ECOPACK(r)2 grade. The permanent evolution of our technology leads us to implement at the same time a die design optimization for our Transil products housed in SMA and SMB packages with voltage inferior to 100V.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	By product marking, QA number and internal codification
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	PCN APM-DIS/09/4781
Please sign and return to STMicroelectronics Sales Office	Notification Date 08/19/2009
Qualification Plan Denied	Name:
Qualification Plan Approved	Title:
	Company:
🗖 Change Denied	Date:
Change Approved	Signature:
Remark	

Name	Function	
Paris, Eric	Division Marketing Manager	
Duclos, Franck	Division Product Manager	
Cazaubon, Guy	Division Q.A. Manager	

DOCUMENT APPROVAL



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-DIS/09/4781

APM - ASD & IPAD Division¹

Protection Devices in SMA/B/C & STmite packages:

Conversion to ECOPACK®2 grade - Die design optimisation of Transils in SMA/B for voltages < 100V



WHY THIS CHANGE?

The ECOPACK® program is the cornerstone of our efforts for being leader in offering **environmentally friendly packaging**. Progressing in this program, ST is implementing technical solutions designed to progressively remove banned substances from manufacturing.

To meet the so called **"Halogen-Free"** requirements of the market, ST is converting its Protection Devices in **SMA/B/C and STmite packages** to the **ECOPACK[®]2** grade.

The permanent evolution of our technology leads us to implement at the same time a **die design optimization** for our **Transil** products housed in **SMA** and **SMB packages** with **voltage inferior to 100V**.

Package	Product series	ECOPACK®2 conversion	Die design optimization	
	SMAJxxA-TR		SMAJ5.0A-TRSMAJ70A-TR	
	SMAJxxCA-TR		SMAJ5.0CA-TRSMAJ70CA-TR	
	SMA6JxxxA-TR		n/a	
SMA	SMA6JxxxCA-TR		n/a	
	SMP30-xxx		n/a	
	SMP50-xxx		n/a	
	SMTYxxxA		n/a	
	LNBTVSxxxU		n/a	
	SM6TxxxA		SM6T6V8A SM6T75A	
	SM6TxxxCA	All	SM6T6V8CA SM6T75CA	
	SMBJxxA-TR		SMBJ5.0A-TRSMBJ70A-TR	
SMB	SMBJxxCA-TR		SMBJ5.0CA-TRSMBJ70CA-TR	
	SMLVT3V3		n/a	
	SMP80-xxx		n/a	
	SMP100-xxx		n/a	
	SMTPAxxx		n/a	
	LNBTVSxxxS		n/a	
	SMCJxxA-TR		n/a	
SMC	SMCJxxCA-TR		n/a	
SIVIC	SM15TxxxA		n/a	
	SM15TxxxCA		n/a	
	SM5908		n/a	
STmite	SM2Txxx		n/a	
STILLE	SMTYxxx		n/a	

The **involved product** series are listed below:

Specific devices not expressly listed in the above table are included in the announced change.

WHAT IS THE CHANGE?

The **ECOPACK[®]2** grade is defined as follows:

- 1. RoHS compliant, including with exemptions,
- 2. **500 ppm** maximum of **Antimony** as oxide or organic compound in each organic assembly materials (glue, substrate, mold compounds, housing).
- 3. **900ppm** maximum of [Bromine + Chlorine], this value referring to the maximum total content.

August 2009

The use of a so-called "**Halogen-free**" moulding compound will have **no impact** on the **dimensional**, **thermal** and intrinsic **electrical parameters of the products** with reference to the product datasheet. This was verified by the qualification program.

For the **Transils** with voltage **inferior to 100V** in **SMA and SMB packages**, the **dice design has been optimized** to take benefit of our last technology developments and design innovations. The **related datasheets** have been updated accordingly as indicated below.

Parameter (SMAJ, SM6T, SMBJ)	Current specification	New specification
Leakage current (> 10V VRм, at 25°С)	< 800nA	< 200nA
Leakage current (> 10V VRM, at 85°C)	Not specified	< 1µA
ESD compliance versus IEC 61000-4-2	Not specified	15kV contact
Dynamic Resistance	Not specified	Specified
Power derating curve above 25°C	No derating up to 25°C	400W no derating up to 65°C 600W no derating up to 120°C

Both changes will be **simultaneously implemented** in the manufacturing sites of **Morocco** and **China**.

There is **no change** in the **packing mode** and in the standard **delivery quantities**.

HOW AND WHEN?

Qualification program and results availability:

The qualification program for each change described above mainly consists of reliability tests and comparative electrical characterizations.

Those qualification reports are annexed to this document.

Samples and characterization data availability:

Qualification samples of selected devices are available on request.

Other samples are available on request for delivery within notice period if ordered within 30 days from notification.

Change implementation schedule:

The **production change** and **first shipments** will be implemented according to our work in progress and materials availability as indicated in the schedule below:

Production Start	1st Shipments	
From Week 35-2009	From Week 47-2009	

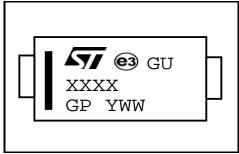
Following Jedec Standard No. 46-C, lack of acknowledgement of the PCN within **30 days** will constitute acceptance of the change. After acknowledgement, lack of additional response within the **90 days** from PCN notification period will constitute acceptance of the change (*). In any case, **first shipments** may start earlier with customer's **written agreement**.

(*) Unless otherwise specified in a customer specific agreement.

Marking and traceability:

When there is room enough on the body of the package, the **marking** of the modified components will be differentiated with an **additional letter** "**G**" that will **be printed to the right of the** "**e3**" symbol specified by IPC-JEDEC J-STD 609 standard (see drawing beside).

The **traceability** for the modified products will be ensured by an **internal codification** and by the **Q.A. number**.



Conversion roadmap:

Deliveries of **current product versions** will continue while the conversion is brought to completion and as long as stocks last.

Annex: Related qualification reports

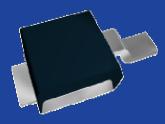
- 07032QRP: Protection devices in STmite package, conversion to halogen-free
- 08198QRP: Protection devices in SMA/SMB/SMC packages assembled in Morocco, conversion to halogen-free
- 08217QRP: Protection devices in SMA/SMB/SMC packages assembled in China, conversion to halogen-free
- **09182QRP**: Transils in SMA/B with voltage < 100V, die design optimization.

QUALIFICATION REPORT

Protection devices and Rectifiers in STmite package: Conversion to halogen-free moulding compound

Author : Didier PELTIER Quality Assurance ST TOURS

Ref:07032QRP Rev:A Date: 23-FEB-2007



REVISION TRACKING

Revision	Date	Description of revision	Name
А	23-Feb-2007	Creation	D.P

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- Reliability evaluation : Tests conditions / Results.
- Average Outgoing Quality level.
- Assessment.

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WHY THIS CHANGE? / WHAT IS THE CHANGE?

Refer to Product Notice Change IMS-DIS/06/STM

Why this change?

In order to meet the global market trend aiming at restricting the Brominated, Chlorinated and Antimony Trioxide based flame retardants, ST announces the conversion of its STmite package epoxy moulding compound to halogen-free.

Such material is considered halogen-free when the concentration of Brominated compound, Chlorinated compound and Sb2O3 are each inferior to 1000 ppm of the plastic weight of the component.

What is the change?

The current epoxy moulding compound EME1100H of Sumitomo will be replaced by the Hysol GR360A, with no other change in the assembly Bill Of Material of the components.

Same test and assembly process will continue to be implemented, with no impact on the mechanical, thermal and electrical parameters of the products with reference to the product datasheets. This was verified in the qualification program.

The product marking will be maintained identical with no change with respect to the compliance with the RoHS* directive. There will be no change in the MSL (moisture sensitivity level 1), packing mode and the standard delivery quantity.

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PRODUCT RANGE

Product	Description	Leakage current	Breakdown voltage	Clamping voltage
SM2T3V3A SM2T6V8A SM2T14A SM2T18A SM2T27A	Transil™ STD 200W unidirectional	Ir < 500μA @ 3.3V Ir < 50μA @ 5V Ir < 1μA @ 12V Ir < 1μA @ 16V Ir < 1μA @ 24V	Vbr > 3.6V @ 1mA Vbr > 6.4V @ 1mA Vbr > 13.3V @ 1mA Vbr > 17.1V @ 1mA Vbr > 25.7V @ 1mA	Vcl < 6.8V @ IPP=30A Vcl < 9.2V @ IPP=19.6A Vcl < 19.9V @ IPP=9A Vcl < 26V @ IPP=7A Vcl < 28.9V @ IPP=4.6A

Product	Description	Leakage current	Forward voltage	Clamping voltage
SMTY18AM	Transky™	4mA @ 16V	Vf < 0.48V @ 0.85A	VcI < 20V @ IPP=1A

Product	Description	Leakage current	Forward voltage
STPS0520M	Power Schottky 0.5A	Ir < 50µA @ 20V	Vf < 0.385V @ 0.5A
STPS1150M STPS120M STPS1L20M STPS1L30M STPS1L40M	Power Schottky 1A	Ir < 1μA @ 150V Ir < 3.9μA @ 20V Ir < 1μA @ 20V Ir < 1μA @ 30V Ir < 1μA @ 40V	Vf < 0.82V @ 1A Vf < 0.49V @ 1A Vf < 0.37V @ 1A Vf < 0.34V @ 1A Vf < 0.40V @ 1A

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Part number	Wafer diameter	Die tech.	Die metallisation (front side)	Die metallisation (back side)
SM2T3V3A			Ti / Tw /Al /Ni /Au	Ti / Ni /Au
SM2T6V8A			Al / Ni / Au	Al / Ni / Au
SM2T14A	(inchos	Planar	Al / Ni / Au	Al / Ni / Au
SM2T18A	6 inches		Al /Ti /Ni /Au	Al / Ni / Au
SM2T27A			Al / Ni / Au	Al / Ni / Au
SMTY18AM			Ti / Tw /Al /Ni /Au	Ti / Ni / Au
STPS0520M STPS1150M STPS120M STPS1L20M STPS1L30M STPS1L40M	5 inches		Al / Ni / Au	Ti / Ni / Au

BASICS OF DIE TECHNOLOGY

DIE / DIFFUSION PLANTS LOCATIONS :

STmicroelectronics TOURS (FRANCE) / STmicroelectronics Ang Mo Kio (SINGAPORE)

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BASICS OF PACKAGE TECHNOLOGY

Part number	Package	Die attach material	Wire bonding material	Frame material	Lead finish material	Molding compound (*)
SM2T3V3A SM2T6V8A SM2T14A SM2T18A SM2T27A SMTY18AM STPS0520M STPS1150M STPS1120M STPS1L20M STPS1L30M STPS1L40M	STmite (JEDEC: DO-216AA)	Soft solder	Bridge (No wire)	Copper	Matte Sn (Lead free)	Epoxy resin GR360A

ASSEMBLY DESCRIPTION

(*): epoxy resin flammability is rated UL94V0

ASSEMBLY / TEST PLANT LOCATION : Subcontractor in China

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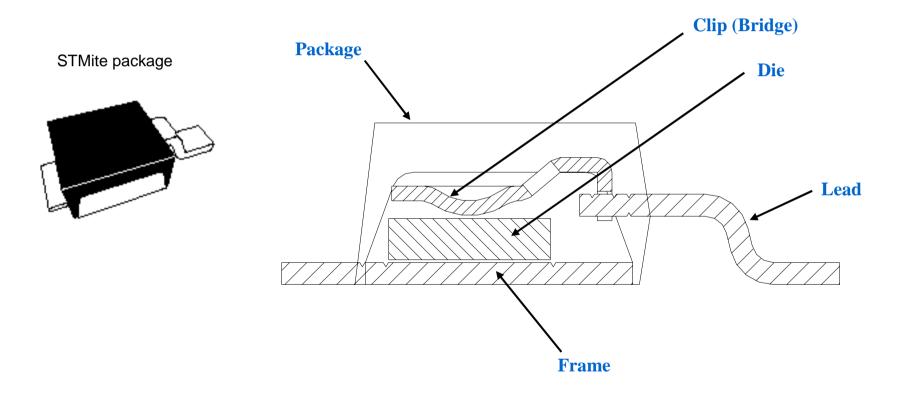
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BASICS OF PACKAGE TECHNOLOGY

INNER ASSEMBLY STRUCTURE



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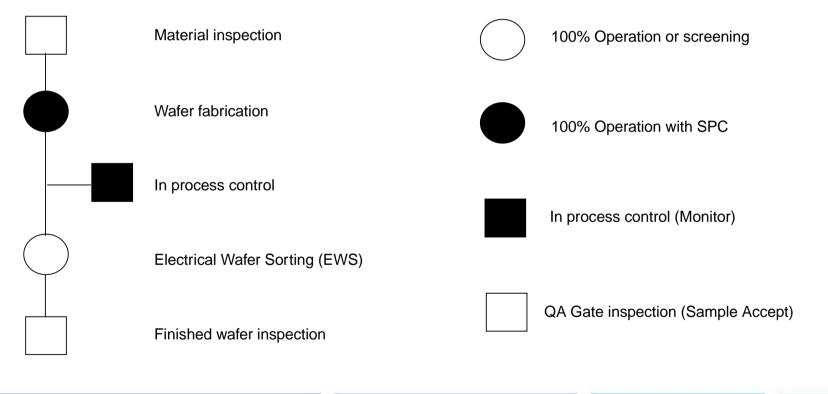
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QC PROCESS FRONT END FLOW CHART

Wafer Fab standard production process flow chart



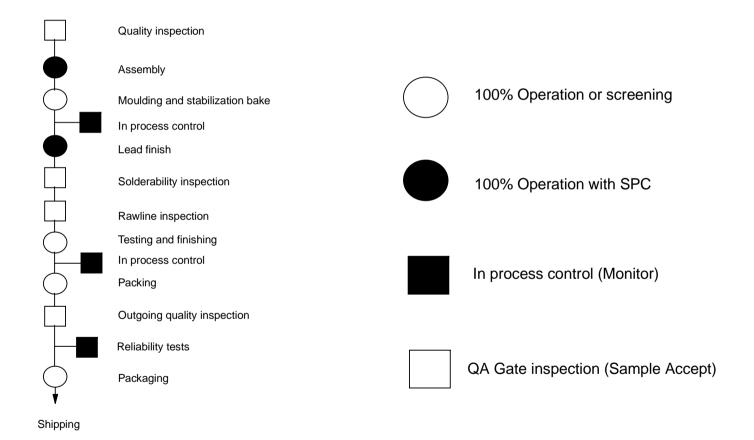
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QC PROCESS BACK END FLOW CHART



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QUALIFICATION PLAN : GUIDELINES AND DESCRIPTION

- * Applicable documents : general procedure SOP2610 (STMicroelectronics). Detail specification : 7923852 (STMicroelectronics).
- * Guidelines : a product or a family of products is considered qualified when it fullfils the requirements of a qualification plan which covers various aspects such as : development, reliability and manufacturing.

RELIABILITY EVALUATION : TEST SELECTION GUIDELINES

Specific emphasis is put on electrical, thermo mechanical and environmental tests which are intended to accelerate failure mechanisms in order to define the limits of the products when they are submitted to industrial conditions.

The tests performed are split into 2 main families called die oriented tests and package oriented tests. Tests are selected according to the knowledge of application conditions of the products, failure mode effect analysis performed at design / development, and to the history of the manufacturing process.

The attached sheets provide relevant information on applicable tests, international standards, failure point, failure process, sample size as well as acceptance numbers.

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RELIABILITY : ABBREVIATIONS AND MEANINGS

* Failure point	: Physical localization of failure.
* Failure process	: Physical or chemical or other mechanism resulting in a failure.
*FIT	: Failure unit ; 1 fit = 1 failure in 10^9 devices - Hours.
* Failure rate	: Also called "Lambda - λ "; it is the incremental change in the number of failures per associated incremental change with time. The failure rate is expressed in fits. Note : MTBF (Mean Time Between Failure) = 1/ λ . Currently " λ " is provided in the life-time of the device (constant λ ; exponential modelisation of the population reliability : R(t) = $N(t) = e^{-\lambda t}$) N(to)
* Accelerating factor	:The physical or chemical factor increasing the failure rate.
•Confidence level	: A 60% confidence level means there is a 60% possibility that the sample came from a population whose failure rate does not exceed the given failure rate.
* Ea	: Activation energy (eV : electron volt). Activation energy is introduced Arrhenius law It is representative of the failure mechanism involved. Ex : 1eV is used to modelize failure rate when surface charges are involved.

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RELIABILITY : DIE ORIENTED TESTS

TEST DESCRIPTIONS	FAILURE POINT	FAILURE PROCESS	ACCELERATING FACTORS / ACTIV. ENERGY
PRECONDITIONING (JESD22A-113) - 24hrs / 125°C - 168hrs / 85%RH / 85°C - 3 IR reflow (260°C max)	PACKAGE HERMETICITY AND DIE VOLUME	POOR HERMETICITY SILICON / PACKAGE	TEMPERATURE AND HUMIDITY SOLDERING SIMULATION
HIGH TEMPERATURE REVERSE BIAS (HTRB) JESD22A-108 1000Hrs, Tj max, VRRM	PASSIVATION LAYERS	SURFACE CHARGES ACCUMULATION	TEMPERATURE ELECTRICAL FIELD Ea = 1.0 eV
OPERATING LIFE TEST (OLT) MIL STD 750C Tj max as specified ; rated forward voltage ; 1000Hrs	ACTIVE AREA AND MECHANICAL INTERFACES	LOCAL THERMAL RUNAWAY	TEMPERATURE CURRENT DENSITY

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RELIABILITY : PACKAGE ORIENTED TESTS

TEST DESCRIPTIONS	FAILURE POINT	FAILURE PROCESS	ACCELERATING FACTORS / ACTIV. ENERGY
PRECONDITIONING (JESD22A-113) - 24hrs / 125°C - 168hrs / 85%RH / 85°C - 3 IR reflow (260°C max)	PACKAGE HERMETICITY AND DIE VOLUME	POOR HERMETICITY SILICON / PACKAGE	TEMPERATURE AND HUMIDITY SOLDERING SIMULATION
THERMAL CYCLING (TCT) JESD22A-104 -55°C/+150°C ; Air / Air ; 1000Cycles	DIE VOLUME DIE ATTACH INTERFACE PASSIVATION LAYERS	SILICON / PACKAGE THERMAL EXPANSION COEFFICIENT MISMATCH	T EXTREMES IN CYCLING.
AUTOCLAVE TEST (PCT) JESD22A-102 133°C ; 3Atm ; 100% RH ; 67Hrs	DIE PERIPHERY PASSIVATION	POOR HERMETICITY CONTAMINATION	TEMPERATURE / PRESSURE
HUMIDITY BIAS (THB) JESD22A-101 85°C 85%RH ; 1000Hrs ; Vbias = Vrm (100V max)	DIE PERIPHERY PASSIVATION BONDS METALLISATION	POOR HERMETICITY CONTAMINATION CORROSION	HUMIDITY TEMPERATURE VOLTAGE Ea=0.8eV
SOLDERABILITY J-STD-002	LEAD SURFACE	PLATING OR DIPPING PROCESS MATERIAL	AGING HUMIDITY TEMPERATURE
RESISTANCE TO SOLDER HEAT 2 oil dipping 260°C 10s ON / 15s OFF	DIE VOLUME	SILICON / PACKAGE	SOLDERING SIMULATION

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RELIABILITY : DIE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER	RESULTS	EXAMPLE OF DRIFT ANALYSIS
HIGH TEMPERATURE REVERSE BIAS (HTRB) After preconditioning JESD22A-108	Tj=150°C, 1000hrs, VR = 0.8 x Vrm	Rectifier diode in SMD package Resin: GR360A Vrm= 1000V	0 / 77	-
		STPS1150M	0 / 77	Refer to graphs #1 and #2
OPERATING LIFE TEST (OLT)	Tj, If as per the datasheet, 1000hrs	Rectifier diode in SMD package Resin: GR360A If= 1A	0 / 77	-

PRECONDITIONING according to JESD22A-113

- 24hrs / 125°C

- 168hrs / 85%RH / 85°C

- 3 IR reflow in oven with recommended T° profile

Note : failure criteria : electrical parameter as defined in product data sheet (*) selected as per structural similarities procedures for CECC 90000 - Issue 4 - Para 3.2.

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RELIABILITY : PACKAGE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER	RESULTS	EXAMPLE OF DRIFT ANALYSIS
PRECONDITIONING +		SM2T18A	0 / 77	-
THERMAL CYCLING (TCT) JESD22A-104	-55°C/+150°C, 1000cycles	Rectifier diode in SMD package Resin: GR360A	0 / 77	-
		SM2T18A	0 / 77	Graphs #3 & #4
PRECONDITIONING +	121°C, 2bars, 96hrs	STPS1150M	0 / 77	Graphs #5 & #6
AUTOCLAVE TEST (PCT) JESD22A-102		Rectifier diode in SMD package Resin: GR360A	0 / 77	-
		SM2T18A	0 / 77	-
PRECONDITIONING + HUMIDITY BIAS (THB)	85°C 85%RH ; V=Vrm (100V max) 1000Hrs	Protection diode in SMD package Resin: GR360A Vrm=33.3V	0 / 77	-
JESD22A-101		Rectifier diode in SMD package Resin: GR360A Vrm= 600V	0 / 77	-

PRECONDITIONING according to JESD22A-113

- 24hrs / 125°C

- 168hrs / 85%RH / 85°C

- 3 IR reflow in oven with recommended T° profile (260°C Max)

Note : failure criteria :electrical parameter as defined in product data sheet

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RELIABILITY : PACKAGE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER	RESULTS
SOLDERABILITY J-STD-002	Solder bath: Sn/Pb 220°C	SM2T18A	Aging A: 0 / 10 Aging B: 0 / 10
 Aging A = 16hrs/150°C (dry air) Aging B = 8hrs/100°C (above boiling water) 	Solder bath: Sn /Ag/Cu 245°C	STPS1150M	Aging A: 0 / 10 Aging B: 0 / 10
RESISTANCE TO SOLDER HEAT (RSH) JESD22B-106-A		SM2T18A STPS1150M	0 / 30 0 / 30
	2 oil dipping 260°C 10s ON / 15s OFF	Protection diode in SMD package Resin: GR360A	0 / 30
		Rectifier diode in SMD package Resin: GR360A	0 / 30

Note : failure criteria :electrical parameter as defined in product data sheet

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RELIABILITY DATA : STATISTICS

In addition to the above table of results, the following graphs provide a straightforward data analysis with a representation of the selected parameter population in the Henry's chart.

Since the "y" axis represents the cumulative population of the different read-outs, statistical analysis is easy (median, range), While in addition the overall stability and span during the stress test is immediately evident.

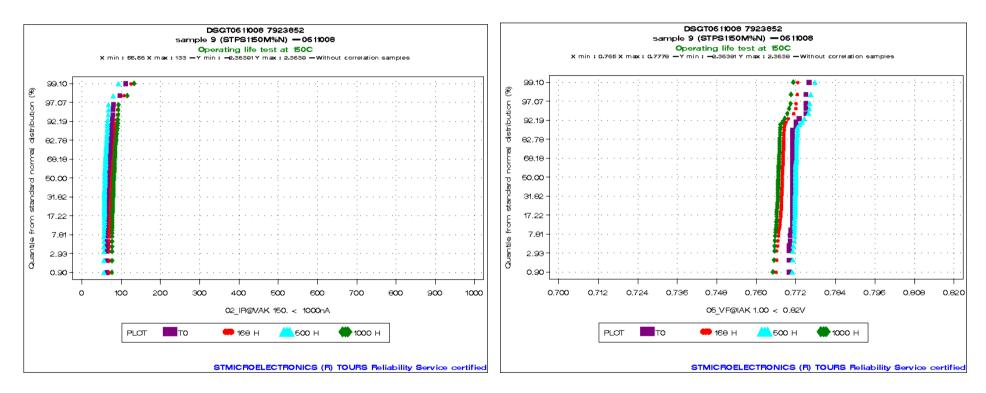
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GRAPHS AND STATISTICS FOR OPERATING LIFE TEST (OLT)



Graph #1 : IR : leakage current

Graph #2 : VF : Forward voltage

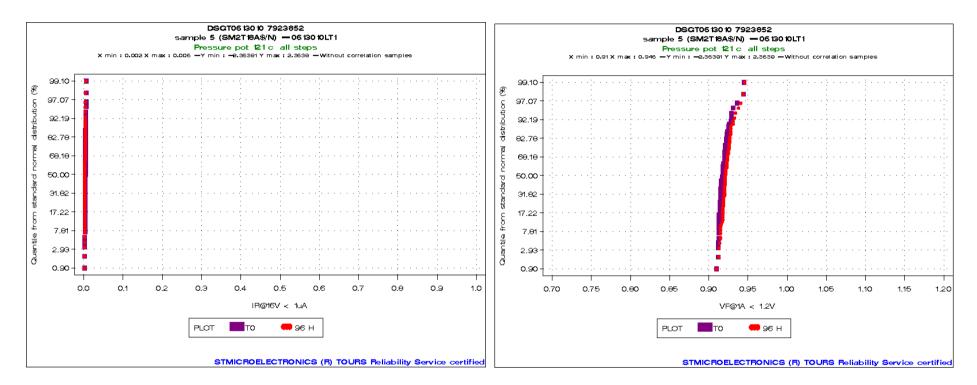
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GRAPHS AND STATISTICS FOR PCT



Graph #3 : IR : leakage current

Graph #4 : VF : Forward voltage

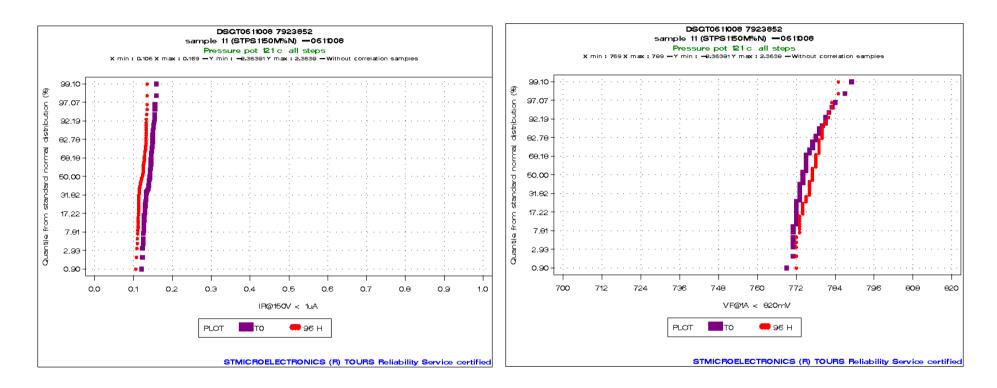
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GRAPHS AND STATISTICS FOR PCT



Graph #5: IR : leakage current

Graph #6 : VF : Forward voltage

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AVERAGE OUTGOING QUALITY LEVEL AT FINAL GATE

Sampling plans at Final quality inspection prior to shipment:

- 200 units per lot for electrical inspection. Acceptance criteria = 0/1
- 315 units per lot for visual and mechanical inspection. Acceptance criteria = 0/1

Ppm calculation:

```
Average Output Quality Estimator = \frac{\text{Total number of defectives on samples with } d \le (c+1)}{\text{Total number of inspected units in accepted lots}} \times 10^{6}
```

where d = defectives on sample c = acceptance criteria

PARAMETER INSPECTED	INSPECTION LEVEL	AQL
VISUAL and MECHANICAL	II	0.04%
ELECTRICAL	II	0.065%

Ref: 070320RP Rev:A Date: 23-FEB-2007



ASSESSMENT

Qualification plan requirements have been fulfilled without exception.

It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their life-time.

Completion date	Location	Department	Name
23-FEB-2007	STMicroelectronics Rue Pierre et Marie CURIE BP155 37071 TOURS Cedex 2, FRANCE	Product Quality Assurance	Didier PELTIER Quality Assurance E-mail : didier.peltier@st.com

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QUALIFICATION REPORT

SMA / SMB /SMC packages in new Halogen-Free Molding Compound Assembly location: Morocco

Author : Didier PELTIER IMS – ASD&IPAD Division Quality Assurance ST Tours

Ref: 08198QRP Rev: C Date: 20-July-09

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REVISION TRACKING

Revision	Date	Description of revision	Name
А	22-Aug-08	Creation	DP
В	24-Feb-09	Add SMA package	DP
С	20-July-09	Add SMC package	DP

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- Qualification plan : Guidelines and description / Reliability tests selection.
- Reliability evaluation : Tests conditions / Results.
- Average Outgoing Quality level.
- Assessment.

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PRODUCT RANGE

Product family	Series				
Protection	SMAJxxx, SMA6Jxxx, SMP30-xxx, SMP50-xxx, SMTYxxx				
	SM6Txxx, SMBJxxx, SMP80xx-xxx, SMP100xx-xxx, SMTPAxxx, SMP75-8				
	SM15Txxx, SMCJxxx, LNBTVSxxx, SM5908	SMC			
Rectifier	STPSxxxxU	SMB			
	STPSxxxA	SMA			
	STPSxxxxS	SMC			
	SMBYxxxx with Vrrm until 400V included	SMB			
	SMBYxxxx with Vrrm until 400V included	SMC			
	STTHxxxxA with Vrrm until 400V included	SMA			
	STTHxxxxU with Vrrm until 400V included	SMB			
	STTHxxxxS with Vrrm until 400V included	SMC			

BASICS OF DIE TECHNOLOGY

Die / diffusion plant locations:

- ST Microelectronics Tours (France)
- ST Ang Mo Kio (Singapore)

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BASICS OF PACKAGE TECHNOLOGY

ASSEMBLY DESCRIPTION

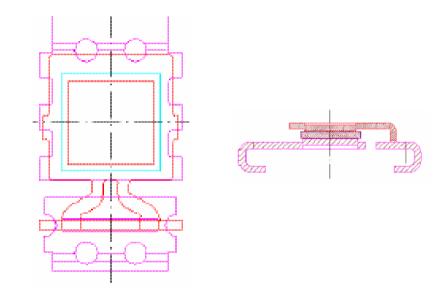
Product family	Die attach material	Bonding material	Frame material	Lead finish material	Package	Molding compound(*)
Protection	Soft solder (Sn/Pb/Ag)	Clip (Copper)	Copper	Sn	SMA SMB SMC	Epoxy resin
Rectifier						

(*): epoxy resin is halogen free and flammability is rated UL94V0



BASICS OF PACKAGE TECHNOLOGY

INNER ASSEMBLY STRUCTURE FOR SMA, SMB and SMC PACKAGE



Note: Generic scheme (Die / wire bonding sizes and die design given as example)

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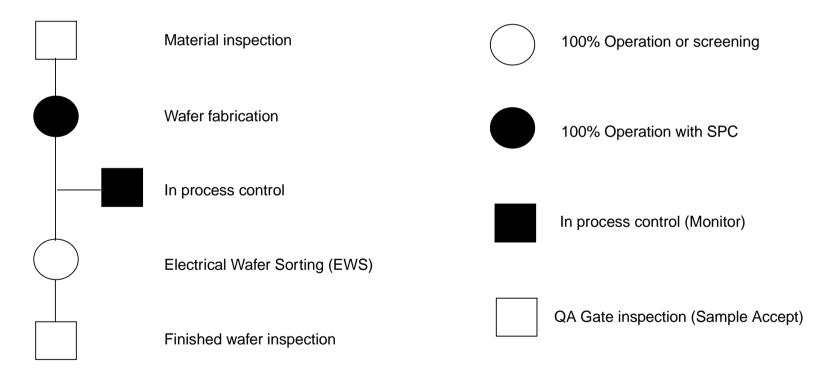
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QC PROCESS FRONT END FLOW CHART

Wafer Fab standard production process flow chart



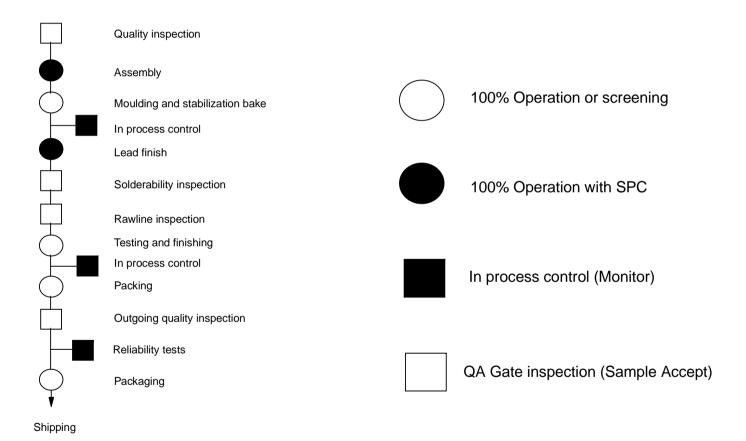
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QC PROCESS BACK END FLOW CHART



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QUALIFICATION PLAN : GUIDELINES AND DESCRIPTION

* Applicable documents : general procedure SOP2610 (STMicroelectronics).

* Guidelines : a product or a family of products is considered qualified when it fullfils the requirements of a qualification plan which covers various aspects such as : development, reliability and manufacturing.

RELIABILITY EVALUATION : TEST SELECTION GUIDELINES

Specific emphasis is put on electrical, thermo mechanical and environmental tests which are intended to accelerate failure mechanisms in order to define the limits of the products when they are submitted to industrial conditions.

The tests performed are split into 2 main families called die oriented tests and package oriented tests. Tests are selected according to the knowledge of application conditions of the products, failure mode effect analysis performed at design / development, and to the history of the manufacturing process.

The attached sheets provide relevant information on applicable tests, international standards, failure point, failure process, sample size as well as acceptance numbers.

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RELIABILITY : ABBREVIATIONS AND MEANINGS

* Failure point	: Physical localization of failure.
* Failure process	: Physical or chemical or other mechanism resulting in a failure.
*FIT	: Failure unit ; 1 fit = 1 failure in 10^9 devices - Hours.
* Failure rate	: Also called "Lambda - λ "; it is the incremental change in the number of failures per associated incremental change with time. The failure rate is expressed in fits. Note : MTBF (Mean Time BetweenFailure) = 1/ λ . Currently " λ " is provided in the life-time of the device (constant λ ; exponential modelisation of the population reliability : R(t) = $N(t) = e^{-\lambda t}$) N(to)
* Accelerating factor	:The physical or chemical factor increasing the failure rate.
 Confidence level 	: A 60% confidence level means there is a 60% possibility that the sample came from a population whose failure rate does not exceed the given failure rate.
* Ea	: Activation energy (eV : electron volt). Activation energy is introduced in Arrhenius law It is representative of the failure mechanism involved. Ex : 1eV is used to modelize failure rate when surface charges are involved.

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RELIABILITY : DIE ORIENTED TESTS

TEST DESCRIPTIONS	FAILURE POINT	FAILURE PROCESS	ACCELERATING FACTORS / ACTIV. ENERGY
HIGH TEMPERATURE REVERSE BIAS (HTRB) JESD22 A-108 For protection, Tj; VR ; 1000Hrs For rectifier: Tj; 0.8xVRRM ; 1000Hrs	PASSIVATION LAYERS	SURFACE CHARGES ACCUMULATION	TEMPERATURE ELECTRICAL FIELD Ea = 1.0 eV
INTERMITENT OPERATING LIFE TEST (IOLT) MIL STD 750C Tj max as specified ; rated forward voltage ; 1000Hrs	ACTIVE AREA AND MECHANICAL INTERFACES	LOCAL THERMAL RUNAWAY	TEMPERATURE CURRENT DENSITY

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RELIABILITY : PACKAGE ORIENTED TESTS

TEST DESCRIPTIONS	FAILURE POINT	FAILURE PROCESS	ACCELERATING FACTORS / ACTIV. ENERGY
THERMAL CYCLING (TCT) JESD22 A-104 -65°C/+150°C ; Air / Air ; 1000Cycles	DIE VOLUME DIE ATTACH INTERFACE PASSIVATION LAYERS	SILICON / PACKAGE THERMAL EXPANSION COEFFICIENT MISMATCH	T EXTREMES IN CYCLING.
AUTOCLAVE TEST (PCT) JESD22 A-102 121°C, 2bars, 100%RH, 96hrs	DIE PERIPHERY PASSIVATION	POOR HERMETICITY CONTAMINATION	TEMPERATURE / PRESSURE
TEMPERATURE HUMIDITY BIAS (THB) JESD22 A-101 85°C 85%RH ; device reverse biased at 0.8xVrrm up to a maximum of 100V ; 1000Hrs	DIE PERIPHERY PASSIVATION BONDS METALLISATION	POOR HERMETICITY CONTAMINATION CORROSION	HUMIDITY TEMPERATURE VOLTAGE Ea=0.8eV
SOLDERABILITY J-STD-002 - Dry aging (150°C, 16Hrs) solderability test 220°C / PbSn - Dry aging (150°C, 16Hrs) solderability test 245°C / SnAgCu - Steam aging (100°C, 8Hrs) solderability test 220°C / PbSn - Steam aging (100°C, 8Hrs) solderability test 245°C / SnAgCu	LEAD SURFACE	PLATING OR DIPPING PROCESS MATERIAL	AGING HUMIDITY TEMPERATURE

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RELIABILITY : DIE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER(*)	RESULTS	EXAMPLE OF DRIFT ANALYSIS
		SM15T200CA	0 / 77	Page 18
HIGH TEMPERATURE REVERSE	For Rectifier	SMBJ5.0A	0 / 86	-
BIAS (HTRB)	Tj , V=0.8xVR, 1000hrs For Protection Tj, V=Vr, 1000hrs	STPS340U	0 / 89	Page 19
JESD22 A-108		STTH112A	0 / 86	-
		SMP100LC-270	0 / 77	-
INTERMITENT OPERATING LIFE	Part powered to reach Δ Tj=100°C,	STPS340U	0 / 86	-
TEST (IOLT)	15000 cycles, 2mn ON, 2mn OFF	STTH112A	0 / 86	Page 20

Note 1: failure criteria :electrical parameter as defined in product data sheet.

(*) selected as per structural similarities procedures for AEC-Q101 standard

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RELIABILITY : PACKAGE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER(*)	RESULTS	EXAMPLE OF DRIFT ANALYSIS
		SM15T200CA	0 / 31	-
THERMAL CYCLING (TCT)	-65°C/+150°C, 1000cycles	SMBJ5.0A	0 / 77	-
JESD22 A-104	-03 C/+130 C, 1000Cycles	STPS340U	0 / 77	Page 21& page 22
		STTH112A	0 / 78	-
		SM15T200CA	0 / 74	-
AUTOCLAVE TEST (PCT) JESD22 A-102	121°C, 2bars, 100%RH, 96hrs	SMBJ5.0A	0 / 77	Page 23
		STPS340U	0 / 77	-
		STTH112A	0 / 79	-

Note 1: failure criteria :electrical parameter as defined in product data sheet.

Note 2: All surface mount devices (SMD's) submitted to pre-conditionning prior reliability test as per JEDEC JESD22-A113.

(*) selected as per structural similarities procedures for AEC-Q101 standard

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RELIABILITY : PACKAGE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER(*)	RESULTS	EXAMPLE OF DRIFT ANALYSIS
	85°C 85%RH; V=0.8xVR (<100V); 1000Hrs	SM15T200CA	0 / 80	Page 24
TEMPERATURE HUMIDITY BIAS		SMBJ5.0A	0 / 77	-
(THB)		STPS340U	0 / 77	Page 25
JESD22 A-101		STTH112A	0 / 80	-

Note 1: failure criteria :electrical parameter as defined in product data sheet.

Note 2: All surface mount devices (SMD's) submitted to pre-conditionning prior reliability test as per JEDEC JESD22-A113. (*) selected as per structural similarities procedures for AEC-Q101 standard.

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RELIABILITY : PACKAGE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER(*)	RESULTS
		SM15T200A	0 / 40 (10 units per test cond.)
	- Dry aging (150°C, 16Hrs) solderability test 220°C / PbSn	SMAJ188CA	0 / 40 (10 units per test cond.)
SOLDERABILITY J-STD-002	 Dry aging (150°C, 16Hrs) solderability test 245°C / SnAgCu Steam aging (100°C, 8Hrs) solderability test 220°C / PbSn Steam aging (100°C, 8Hrs) solderability test 245°C / SnAgCu 	SMBJ5.0A	0 / 40 (10 units per test cond.)
		STPS340U	0 / 40 (10 units per test cond.)
			0 / 40 (10 units per test cond.)
			0 / 500
IR REFLOW J-STD-020C	3 time with IR Reflow 260°C max (lead free profile)	STTH112A	0 / 500
0.010.0200		SMBJ5.0A	0 / 500

Note 1: failure criteria :electrical parameter as defined in product data sheet.

Note 2: All surface mount devices (SMD's) submitted to pre-conditionning prior reliability test as per JEDEC JESD22-A113. (*) selected as per structural similarities procedures for AEC-Q101 standard

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RELIABILITY DATA : STATISTICS

In addition to the above table of results, the following graphs provide a straightforward data analysis with a representation of the selected parameter population in the Henry's chart.

Since the « y » axis represents the cumulative population of the different read-outs, statistical analysis is easy (median, range), while the overall stability and span during the stress test is immediately evident.

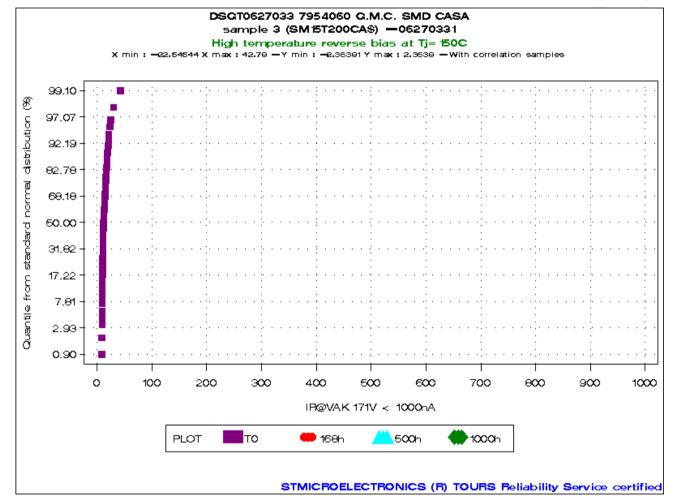
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GRAPHS AND STATISTICS FOR HIGH TEMPERATURE REVERSE BIAS (HTRB)



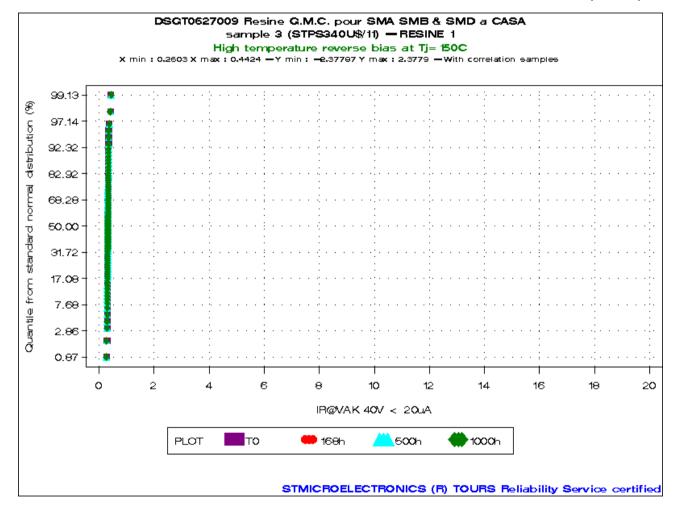
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GRAPHS AND STATISTICS FOR HIGH TEMPERATURE REVERSE BIAS (HTRB)



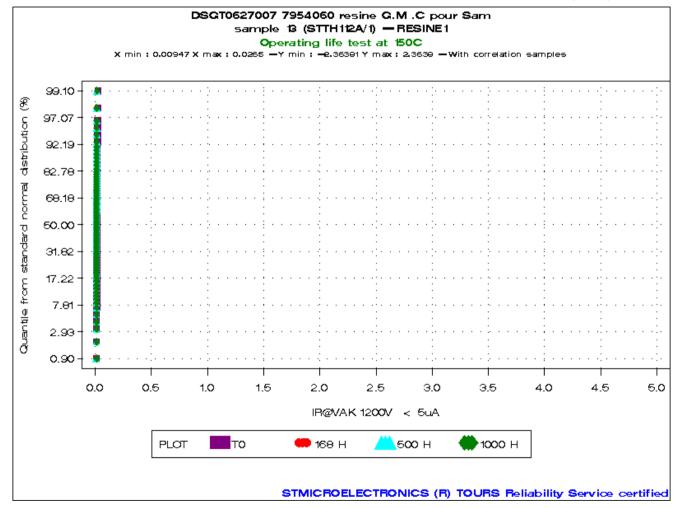
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GRAPHS AND STATISTICS FOR INTERMITENT OPERATING LIFE TEST (OLT)



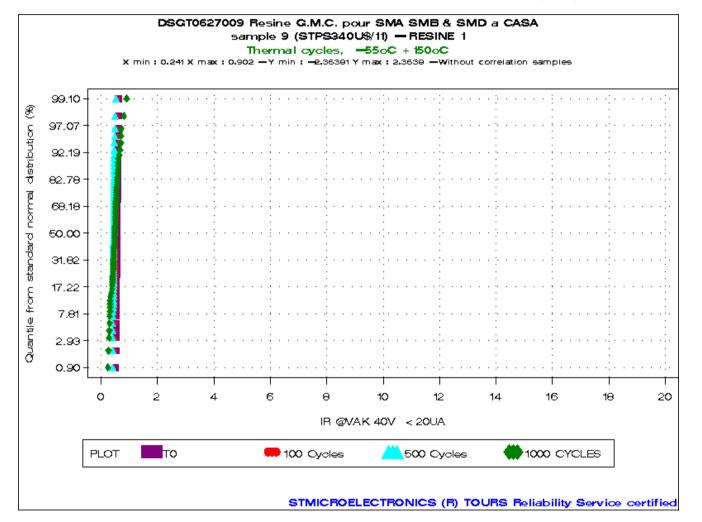
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GRAPHS AND STATISTICS FOR THERMAL CYCLING (TCT)



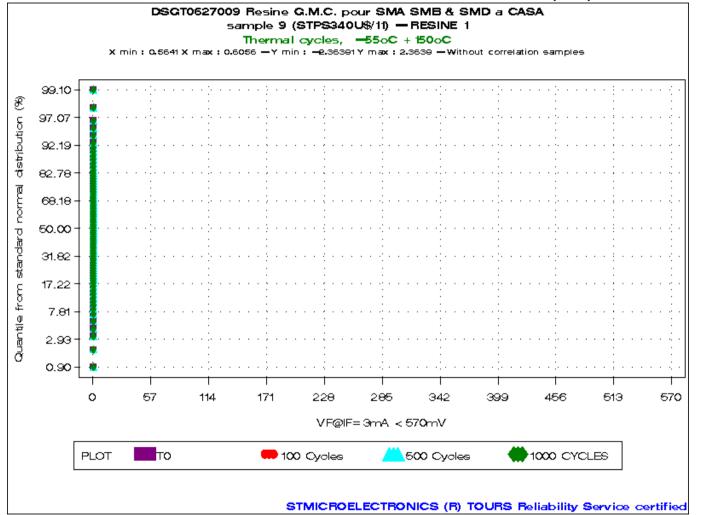
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GRAPHS AND STATISTICS FOR THERMAL CYCLING (TCT)



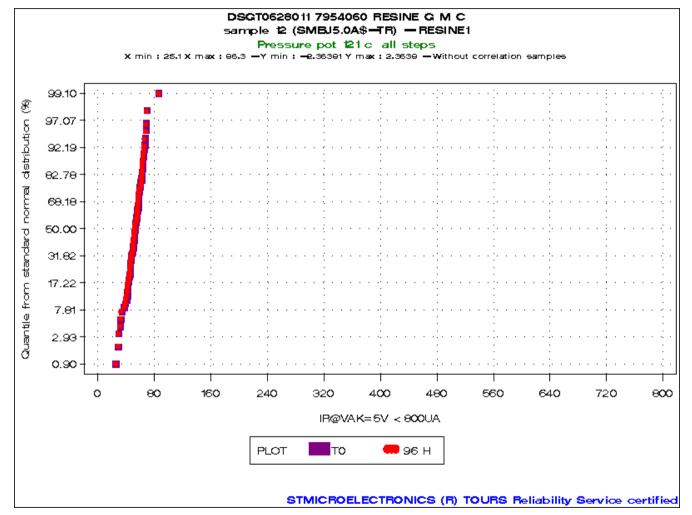
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GRAPHS AND STATISTICS FOR AUTOCLAVE TEST (PCT)



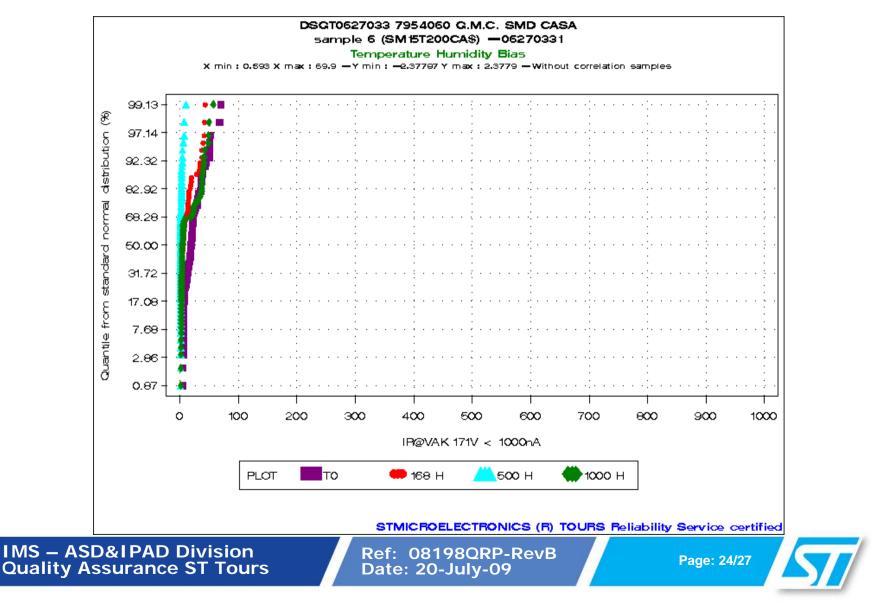
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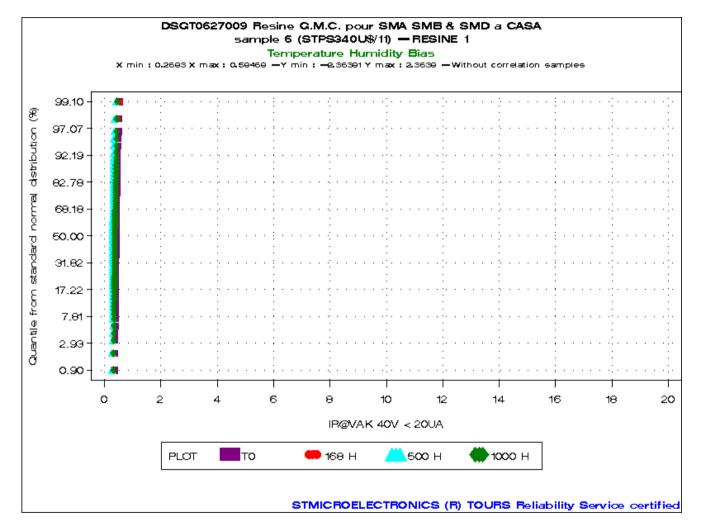
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GRAPHS AND STATISTICS FOR THB



GRAPHS AND STATISTICS FOR THB



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AVERAGE OUTGOING QUALITY LEVEL AT FINAL GATE

Sampling plans at Final quality inspection prior to shipment:

- 200 units per lot for electrical inspection. Acceptance criteria = 0/1
- 315 units per lot for visual and mechanical inspection. Acceptance criteria = 0/1

Ppm calculation:

Average Output Quality Estimator = $\frac{\text{Total number of defectives on samples with } d \le (c+1)}{\text{Total number of inspected units in accepted lots}} \times 10^6$

where d = defectives on sample c = acceptance criteria

PARAMETER INSPECTED	INSPECTION LEVEL	AQL
VISUAL and MECHANICAL	II	0.04%
ELECTRICAL	II	0.065%

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ASSESSMENT

AEC-Q101 Qualification Plan requirements have been fulfilled without exception.

It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Completion date	Location	Department	Name
July 20th, 2009	STMicroelectronics Rue Pierre et Marie CURIE BP155 37071 TOURS Cedex 2, FRANCE	Product Quality Assurance	Didier PELTIER Quality Assurance Products E-mail : didier.peltier@st.com

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QUALIFICATION REPORT

SMD package in new Halogen-Free molding compound

Assembly location: Subcontractor in China

Author : Didier PELTIER IMS – ASD&IPAD Division Quality Assurance ST Tours

Ref: 08217QRP Rev: A Date: 24-Oct-2008

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REVISION TRACKING

Revision	Date	Description of revision	Name
А	24-Oct-2008	Creation	DP

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Ref: 08217QRP-RevA Date: 24-Oct-2008

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CONTENTS

- Why this change
- Product range.
- Basics of die technology.
- Basics of package technology.
- QC process flow chart.
- Qualification plan : Guidelines and description / Reliability tests selection.
- Reliability evaluation : Tests conditions / Results.
- Average Outgoing Quality level.
- Assessment.

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WHY THIS CHANGE

Why this change?

In order to meet the global market trend aiming at restricting the Brominated, Chlorinated and Antimony Trioxide based flame retardants, ST announces the conversion of its SMD package epoxy moulding compound to halogen-free.

Such material is considered halogen-free when the concentration of Brominated compound, Chlorinated compound and Sb2O3 are each inferior to 1000 ppm of the plastic weight of the component.

What is the change?

The current epoxy moulding compound will be replaced by the halogen-free molding compound with no other change in the assembly Bill Of Material of the components.

Same test and assembly process will continue to be implemented, with no impact on the mechanical, thermal and electrical parameters of the products with reference to the product datasheets. This was verified in this qualification program.

The product marking will be maintained identical with no change with respect to the compliance with the RoHS* directive. There will be no change in the MSL (moisture sensitivity level 1), packing mode and the standard delivery quantity.

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PRODUCT RANGE

Package	Product family	Series
<u>CMA</u>	Protection	SMAJxxx,
SMA	Rectifier	STPSxxxA, STTHxxxA
CMD	Protection	SMBJxxx, SM6Txxx,
SMB	Rectifier	SMBYTxxx, STPSxxxU, STPSxxxS
SMC	Protection	SMCJxxx, SM15Txxx, LNBTVSxxxS
SIVIC	Rectifier	SMBYTxxx, STPSxxxS, STPSxxxS

BASICS OF DIE TECHNOLOGY

Die / diffusion plant locations:

- ST Microelectronics Tours (France)
- ST Ang Mo Kio (Singapore)

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BASICS OF PACKAGE TECHNOLOGY

ASSEMBLY DESCRIPTION

Product family	Die attach material	Bonding material	Frame material	Lead finish material	Package	Molding compound(*)
Protection	Soft solder (Sn/Pb/Ag)	Clip (Copper)	Copper	Sn	SMA SMB SMC	Epoxy resin
Rectifier						

(*): epoxy resin is halogen free and flammability is rated UL94V0



ASSEMBLY / TEST PLANT LOCATION : Subcontractor in China

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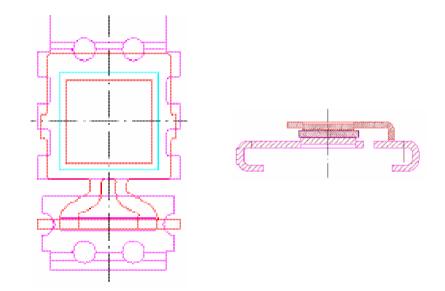
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BASICS OF PACKAGE TECHNOLOGY

INNER ASSEMBLY STRUCTURE



Note: Generic scheme (Die / wire bonding sizes and die design given as example)

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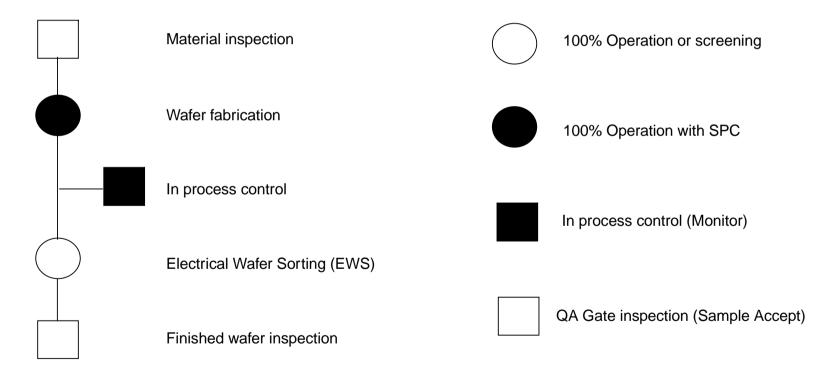
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QC PROCESS FRONT END FLOW CHART

Wafer Fab standard production process flow chart



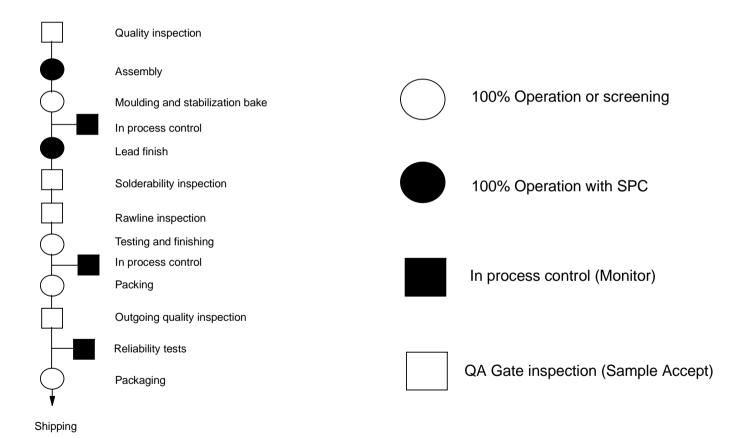
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QC PROCESS BACK END FLOW CHART



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QUALIFICATION PLAN : GUIDELINES AND DESCRIPTION

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RELIABILITY : ABBREVIATIONS AND MEANINGS

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* Failure process	: Physical or chemical or other mechanism resulting in a failure.
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* Failure rate	: Also called "Lambda - λ "; it is the incremental change in the number of failures per associated incremental change with time. The failure rate is expressed in fits. Note : MTBF (Mean Time BetweenFailure) = 1/ λ . Currently " λ " is provided in the life-time of the device (constant λ ; exponential modelisation of the population reliability : R(t) = $N(t) = e^{-\lambda t}$) N(to)
* Accelerating factor	:The physical or chemical factor increasing the failure rate.
•Confidence level	: A 60% confidence level means there is a 60% possibility that the sample came from a population whose failure rate does not exceed the given failure rate.
* Ea	: Activation energy (eV : electron volt). Activation energy is introduced in Arrhenius law It is representative of the failure mechanism involved. Ex : 1eV is used to modelize failure rate when surface charges are involved.

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RELIABILITY : DIE ORIENTED TESTS

TEST DESCRIPTIONS	FAILURE POINT	FAILURE PROCESS	ACCELERATING FACTORS / ACTIV. ENERGY
HIGH TEMPERATURE REVERSE BIAS (HTRB) JESD22 A-108 For protection, Tj; VR ; 1000Hrs For rectifier: Tj; 0.8xVRRM ; 1000Hrs	PASSIVATION LAYERS	SURFACE CHARGES ACCUMULATION	TEMPERATURE ELECTRICAL FIELD Ea = 1.0 eV

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RELIABILITY : PACKAGE ORIENTED TESTS

TEST DESCRIPTIONS	FAILURE POINT	FAILURE PROCESS	ACCELERATING FACTORS / ACTIV. ENERGY
THERMAL CYCLING (TCT) JESD22 A-104 -65°C/+150°C ; Air / Air ; 1000Cycles	DIE VOLUME DIE ATTACH INTERFACE PASSIVATION LAYERS	SILICON / PACKAGE THERMAL EXPANSION COEFFICIENT MISMATCH	T EXTREMES IN CYCLING
AUTOCLAVE TEST (PCT) JESD22 A-102 121°C, 2bars, 100%RH, 96hrs	DIE PERIPHERY PASSIVATION	POOR HERMETICITY CONTAMINATION	TEMPERATURE / PRESSURE
TEMPERATURE HUMIDITY BIAS (THB) JESD22 A-101 85°C 85%RH ; device reverse biased at 0.8xVrrm up to a maximum of 100V ; 1000Hrs	DIE PERIPHERY PASSIVATION BONDS METALLISATION	POOR HERMETICITY CONTAMINATION CORROSION	HUMIDITY TEMPERATURE VOLTAGE Ea=0.8eV
SOLDERABILITY J-STD-002	LEAD SURFACE	PLATING OR DIPPING PROCESS MATERIAL	AGING HUMIDITY TEMPERATURE
RESISTANCE TO SOLDER HEAT (RSH) JESD22 B-106-A	DIE VOLUME DIE ATTACH INTERFACE PASSIVATION LAYERS	SILICON / PACKAGE THERMAL EXPANSION COEFFICIENT MISMATCH	TEMPERATURE EXTREME

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RELIABILITY : DIE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER(*)	RESULTS	EXAMPLE OF DRIFT ANALYSIS
HIGH TEMPERATURE REVERSE BIAS (HTRB) JESD22 A-108	For Rectifier Tj , V=0.8xVR, 1000hrs For Protection Tj, V=Vr, 1000hrs	SM6T68A	0 / 77	Refer to graph #1
		LNBTVS-6-304S	0 / 77	-
		STTH310S	0 / 77	Refer to graph #2

Note 1: failure criteria :electrical parameter as defined in product data sheet.

(*) selected as per structural similarities procedures according to AEC-Q101.

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RELIABILITY : PACKAGE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER(*)	RESULTS	EXAMPLE OF DRIFT ANALYSIS	
THERMAL CYCLING (TCT) JESD22 A-104	-65°C/+150°C, 500cycles	LNBTVS6-304S	0 / 77	Refer to graph #3	
U-HAST TEST JESD22A-110-B			-		
	130°C / 100%RH / 96Hrs		Refer to graph #4		
			0 / 25	Refer to graph #5	
TEMPERATURE HUMIDITY BIAS (THB) JESD22 A-101	85°C 85%RH; V=0.8xVR	SM6T68A	0 / 25	Refer to graph #6	
	(<100V); 1000Hrs	STTH1L06A	0 / 25	Refer to graph #7	
		LNBTVS6-304S	0 / 25	-	

Note 1: failure criteria :electrical parameter as defined in product data sheet.

Note 2: All surface mount devices (SMD's) submitted to pre-conditionning prior reliability test as per JEDEC JESD22-A113.

(*) selected as per structural similarities procedures according to AEC-Q101.

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RELIABILITY : PACKAGE ORIENTED TESTS CONDITIONS / RESULTS

RELIABILITY TEST	TEST CONDITIONS	RUNNER(*)	RESULTS
	- Dry aging (150°C, 16Hrs) solderability test 220°C / PbSn	SMAJ33CA	0 / 60
SOLDERABILITY J-STD-002	 Dry aging (150°C, 16Hrs) solderability test 245°C / SnAgCu Steam aging (100°C, 8Hrs) solderability test 220°C / PbSn Steam aging (100°C, 8Hrs) solderability test 245°C / SnAgCu 	SM6T68A	0 / 60
		LNBTVS6-304S	0 / 60
RSH (Resistance	er Heat) T = 260°C / 10s ON / 15s OFF (2 times)	SMAJ33CA	0 / 12
to Solder Heat) JESD22 B-106-A		SM6T68A	0 / 12
		LNBTVS6-304S	0 / 12

Note 1: failure criteria :electrical parameter as defined in product data sheet.

Note 2: All surface mount devices (SMD's) submitted to pre-conditionning prior reliability test as per JEDEC JESD22-A113.

(*) selected as per structural similarities procedures according to AEC-Q101.

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RELIABILITY DATA : STATISTICS

In addition to the above table of results, the following graphs provide a straightforward data analysis with a representation of the selected parameter population in the Henry's chart.

Since the « y » axis represents the cumulative population of the different read-outs, statistical analysis is easy (median, range), while the overall stability and span during the stress test is immediately evident.

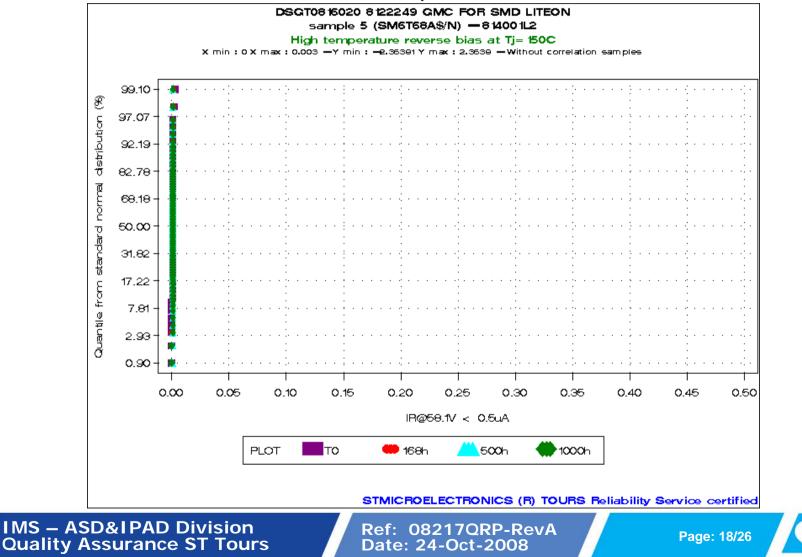
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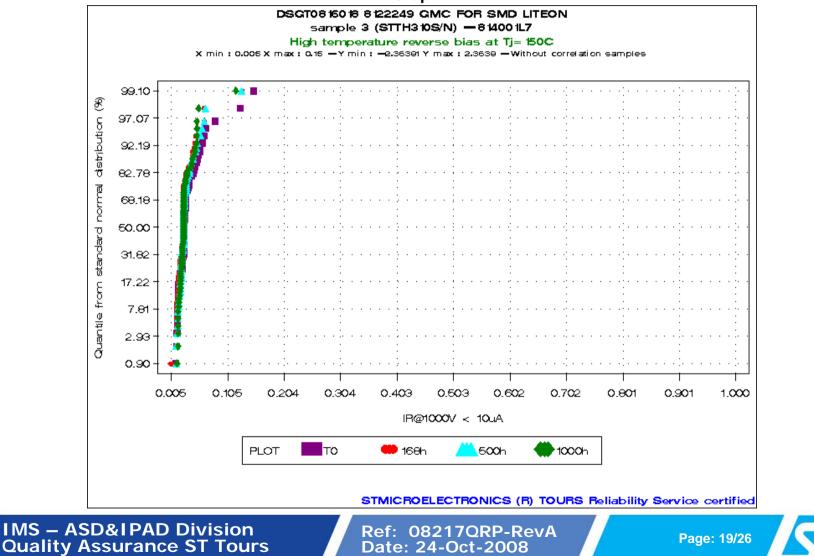
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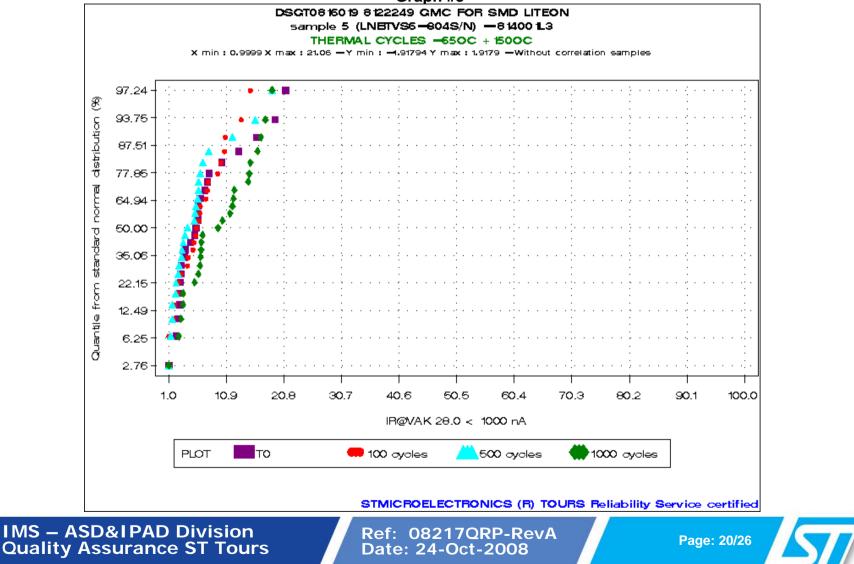
GRAPHS AND STATISTICS FOR HIGH TEMPERATURE REVERSE BIAS (HTRB)



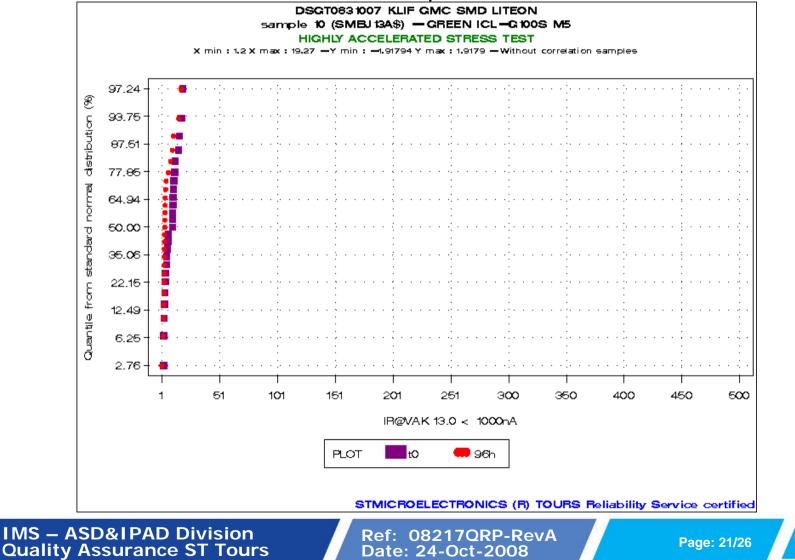
GRAPHS AND STATISTICS FOR HIGH TEMPERATURE REVERSE BIAS (HTRB)



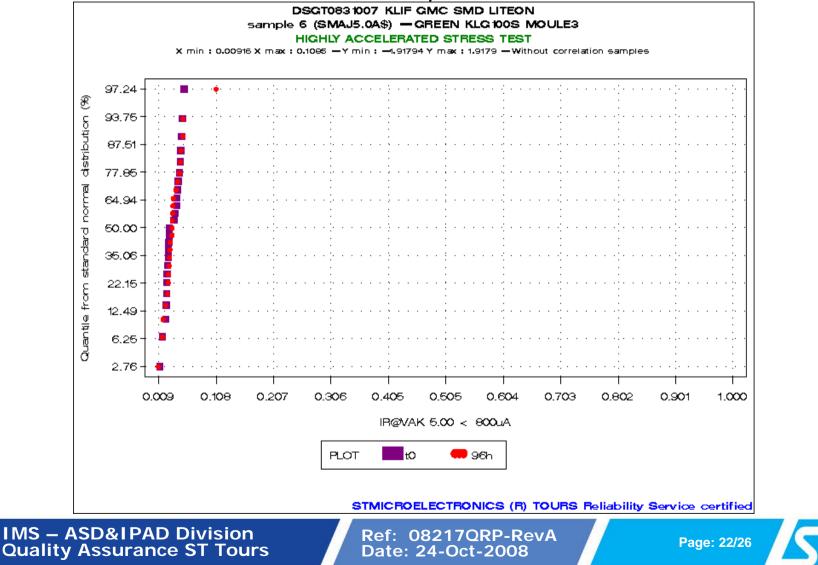
GRAPHS AND STATISTICS FOR THERMAL CYCLING (TCT)



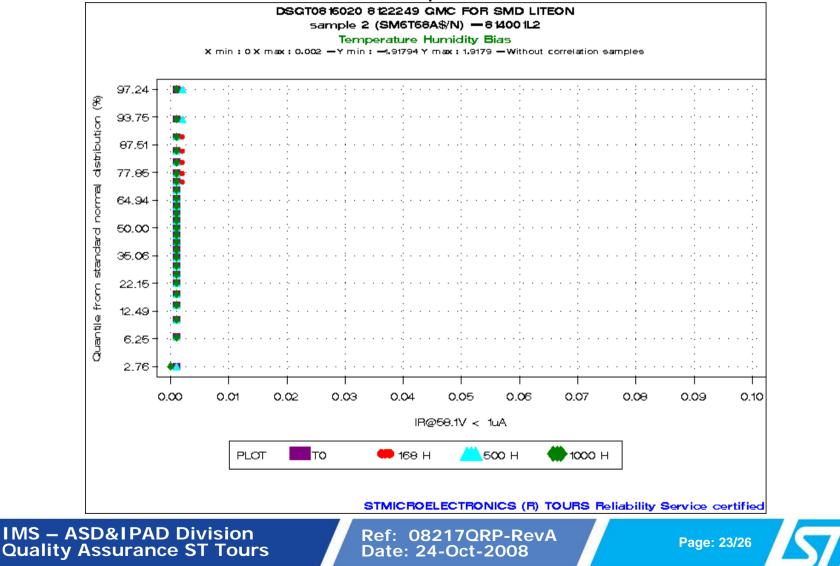
GRAPHS AND STATISTICS FOR U-HAST



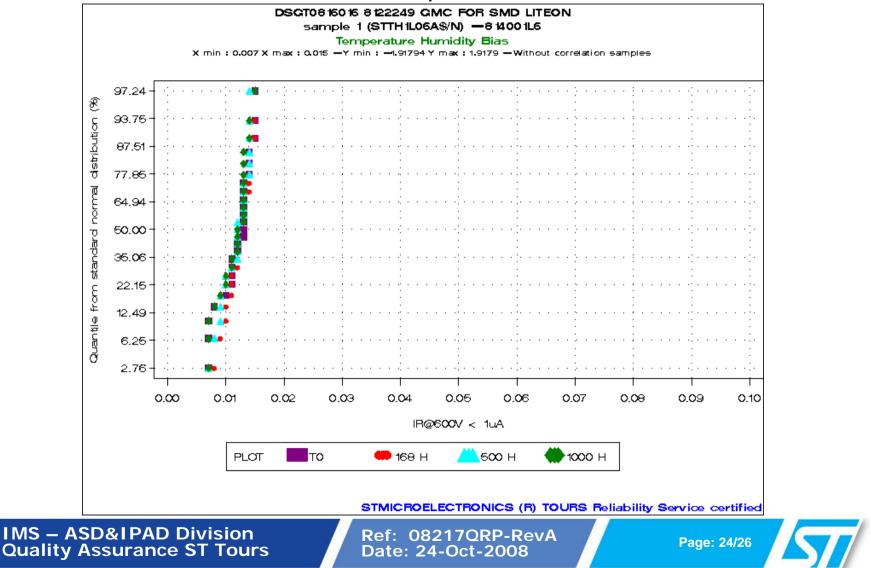
GRAPHS AND STATISTICS FOR U-HAST



GRAPHS AND STATISTICS FOR THB



GRAPHS AND STATISTICS FOR THB



AVERAGE OUTGOING QUALITY LEVEL AT FINAL GATE

Sampling plans at Final quality inspection prior to shipment:

- 200 units per lot for electrical inspection. Acceptance criteria = 0/1
- 315 units per lot for visual and mechanical inspection. Acceptance criteria = 0/1

Ppm calculation:

Average Output Quality Estimator = $\frac{\text{Total number of defectives on samples with } d \le (c+1)}{\text{Total number of inspected units in accepted lots}} \times 10^6$

where d = defectives on sample c = acceptance criteria

PARAMETER INSPECTED	INSPECTION LEVEL	AQL
VISUAL and MECHANICAL	II	0.04%
ELECTRICAL	II	0.065%

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ASSESSMENT

AEC-Q101 Qualification Plan requirements have been fulfilled without exception.

It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Completion date	Location	Department	Name
Oct 24th, 2008	STMicroelectronics Rue Pierre et Marie CURIE BP155 37071 TOURS Cedex 2, FRANCE	Product Quality Assurance	Didier PELTIER Quality Assurance Products E-mail : didier.peltier@st.com

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Die layout optimization for transilTM standard

General In	formation		Locations
Product Line Product Description	Transil standard Devices designed specifically for protection sensitive equipment against transient	Wafer fab	STMicroelectronis Tours (France)
P/N	electrical overstress. Refer to table of involved products (Paragraph 3.1)	Assembly plant	- STMicroelectronics Bouskoura (MOROCCO) - Subcontractor in CHINA
Product Group Product division Package Silicon Process technology Maturity level step	APM ASD & IPAD SMA and SMB Transil planar 30	Reliability Lab	STMicroelectronis Tours (FRANCE)

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	07-Nov-2008	9	D.PELTIER	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.



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<u>1</u> APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description		
AEC-Q100	Stress test qualification for automotive grade integrated circuits		
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors		
JESD47	Stress-Test-Driven Qualification of Integrated Circuits		

2 GLOSSARY

DUT	Device Under Test	
PCB	Printed Circuit Board	
SS	Sample Size	

3 RELIABILITY EVALUATION OVERVIEW

<u>3.1</u> Objectives

Qualification of die layout optimization on the following products:

Product	Package
SMAJ5.0A-TRSMAJ70A-TR SMAJ5.0CA-TRSMAJ70CA-TR	SMA
SM6T6V8A SM6T75A SM6T6V8CA SM6T75CA SMBJ5.0A-TRSMBJ70A-TR SMBJ5.0CA-TRSMBJ70CA-TR	SMB

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



4 DEVICE CHARACTERISTICS

4.1 Device description

Devices designed specifically for protection sensitive equipment against transient electrical overstress.

4.2 Construction note

	Transil standard
Wafer/Die fab. information	
Wafer fab manufacturing location	STMicroelectronics Tours (France)
Technology	Planar
Process family	Transil standard
Die finishing back side	Al / Ni / Au
Die size	SMAJxxxx: 1.25mm x 1.25mm x 300µm SMBJxxxx and SM6Txxxx: 1.5mm x 1.5mm x 300µm
Bond pad metallization layers	Au
Passivation type	SiO ₂
Assembly information	
Assembly site	STMicroelectronics Bouskoura (Morocco) / Subcontractor in China
Package description	SMA / SMB
Molding compound	Green epoxy resin
Frame material	Copper
Die attach material	Soft solder paste
Wire bonding process	N/A as clip used
Wires bonding materials/diameters	N/A as clip used
Lead finishing process	Sn 100% (Lead free)
Final testing information	
Testing location	STMicroelectronics Bouskoura (Morocco) / Subcontractor in China



5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Product	Die process	Package
SMAJ5.0A-TR	Uni-directional transil planar	SMA
SMAJ13A-TR	Uni-directional transil planar	SMA
SMAJ33A-TR	Uni-directional transil planar	SMA
SMAJ33CA-TR	Bi-birectional transil planar	SMA
SMAJ58CA-TR	Bi-birectional transil planar	SMA
SMBJ5.0A-TR	Uni-directional transil planar	SMB
SMBJ13A-TR	Uni-directional transil planar	SMB
SMBJ33CA-TR	Bi-birectional transil planar	SMB
SMBJ58CA-TR	Bi-birectional transil planar	SMB
SMBJ33A-TR	Uni-directional transil planar	SMB
SM6T36CA	Bi-birectional transil planar	SMB
SM6T68A	Uni-directional transil planar	SMB

5.2 Test plan and results summary

SMAJ58CA-TR

	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Orien	tea	Tests		1		a (a a	
Repetitive					100surges	0/20	
Surge	Y	ADCS0060282	IPP=4.3A/us, waveform 10/1000us	20	500surges	0/20	
Ourge					1000surges	0/20	

SMBJ33A-TR

Test	РС	Std ref.	Conditions	SS	Steps	Failure/SS	Note
					-	Lot 1	
Die Orien	ted	Tests					
Repetitive					100surges	0/20	
Surge	Υ	DCS0060282	IPP =11.8A/µs, waveform 10/1000us	20	500surges	0/20	
Ourge					1000surges	0/20	

SMBJ33CA-TR

Test	РС	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Orien	ted [·]	Tests			11	2011	
Donotitivo					100surges	0/20	
Repetitive Surge	Υ	DCS0060282	IPP 11.8A/us, waveform 10/1000us	20	500surges	0/20	
Ourge					1000surges	0/20	



SM6T68A

Test	РС	Std ref.	Conditions	SS	Steps	Failure/SS	Note
1631	10	Sturiei.	Conditions	55	Oteps	Lot 1	Note
Die Orien	ted	Tests					-
Popotitivo					100surges	0/20	
Repetitive Surge	Υ	DCS0060282	IPP = 6.5A/us, waveform 10/1000us	20	500surges	0/20	
Surge					1000surges	0/20	

SMBJ58CA-TR

Test	РС	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Orien [®]	ted	Tests					
Repetitive					100surges	0/20	
Surge	Υ	DCS0060282	IPP = 6.7 A/us, waveform 10/1000us	20	500surges	0/20	
Cargo					1000surges	0/20	

SMAJ33A-TR

Test	РС	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Orien	ted	Tests					
Dopotitivo					100surges	0/20	
Repetitive Surge	Υ	DCS0060282	IPP =11.8A/µs, waveform 10/1000us	20	500surges	0/20	
Ourge					1000surges	0/20	

SMAJ33CA-TR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Orien	ted	Tests			-		
Popotitivo					100surges	0/20	
Repetitive Surge	Υ	DCS0060282	IPP =11.8A/µs, waveform 10/1000us	20	500surges	0/20	
Carge					1000surges	0/20	

SMAJ58CA-TR

Test	РС	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Orien	ted	Tests					
Repetitive					100surges	0/20	
Surge	Υ	DCS0060282	IPP = 6.7 A/us, waveform 10/1000us	20	500surges	0/20	
Ourge					1000surges	0/20	

SM6T68A / SMBJ5.0A-TR

Test	РС	Std ref.	Conditions	SS	Steps	Fai	Note	
1631	FC			33	Oteps	SM6T68A	SMBJ5.0A-TR	NOLE
Die Orien	ted	Tests						
		JESD22			168 H	0/77	0/86	
HTRB	Ν	A-108	Tj = 150°C, V=Vr	231	500 H	0/77	0/86	
		A 100			1000 H	0/77	0/86	



SMAJ33A-TR

Test	РС	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Package Orien	ted	Tests		-			
тс	v	JESD22 A-	-65°C +150°C, 2	25	100 cycles	0/25	
10	I	104	cycles/hour	23	500 cycles	0/25	

SMAJ13A-TR / SM6T36CA

Test	РС	Std ref.	Conditions	SS	Steps	Failu	re/SS	Note
1631			Steps	SMAJ13A-TR	SM6T36CA	NOLE		
Package Orien	ted T	ests						
AC	Υ	JESD22 A- 102c	T=133°C, HR=100% P=2Bars	77	67h	0/77	0/77	
		JESD22 A-	T=85°C HR=85%		168h	0/20	0/20	
THB	Y	101	V= Vr	25	504h	0/20	0/20	
			V = VI		1000h	0/20	0/20	

SMAJ5.0A-TR

Tost	Test PC Std ref. Conditions SS		99	Steps	Fa	ailure/S	Note		
Test			3	Steps	Lot 1	Lot 2	Lot 3	Note	
Package	Orie	nted Tests							
AC	Υ	JESD22 A-102	T=121°C, HR=100% P=2Bars	75	96 H	0/25	0/25	0/25	

SMBJ13A-TR

Test	PC	Std ref.	Conditions	SS	Steps	Failu Lot 1	re/SS Lot 2	Note
Package Oriented Tests								
AC	Υ	JESD22 A-102	T=121°C, HR=100% P=2Bars	50	96 H	0/25	0/25	

SMAJ5.0A-TR

Test PC	PC	C Std ref.	Conditions	SS	Steps	Failure/SS			Note
	FC		Conditions			Lot 1	Lot 2	Lot 3	Note
Package Oriented Tests									
u-HAST	Υ	JESD22 A-102	T=133°C, HR=85%	75	96 H	0/25	0/25	0/25	

SMBJ13A-TR

Test PC	BC	C Std ref.	Conditions	SS Step	Stone	Failure/SS		Note
	FC		Conditions		Steps	Lot 1	Lot 2	Note
Package Oriented Tests								
u-HAST	Υ	JESD22 A-102	T=133°C, HR=85%	50	96 H	0/25	0/25	



6 ANNEXES

6.1 Device details

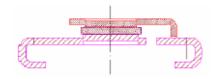
6.1.1 Pin connection



Unidirectional

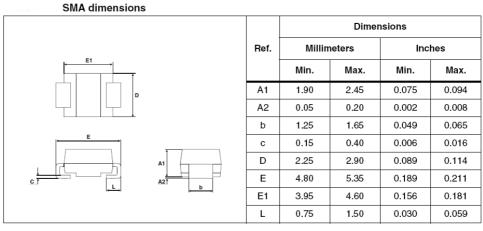
For unidirectional units, there is a cathode band on the package

6.1.2 Bonding diagram

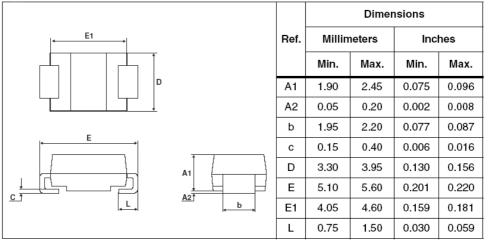


Bidirectional

6.1.3 Package outline/Mechanical data



SMB package dimensions





6.2 Tests Description

Test name	Description	Purpose							
Die Oriented									
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.							
Package Oriented									
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.							
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.							
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.							
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.							

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