PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-PWR/09/4736
Notification Date 07/21/2009

SILICON LINE CHANGE FOR BIPOLAR DEVICES - BD03 PRODUCT LINE

Table 1. Change Implementation Schedule

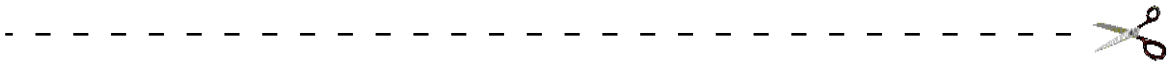
Forecasted implementation date for change	14-Oct-2009
Forecasted availabillity date of samples for customer	14-Jul-2009
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	14-Jul-2009
Estimated date of changed product first shipment	20-Oct-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Waferfab process change
Reason for change	Production Optimization
Description of the change	Planar Base Island technology is ready to replace the mature Epibase technology in order to align our products to the actual Market. The line BD03 will replace the old ones B215. Feature: Improved hFE linearity and Higher fT frequency. Benefit: Better performances in switching and linear application.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	See "N" in additional info
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM-PWR/09/4736**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 07/21/2009**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Saya, Francesco	Division Marketing Manager
Aleo, Mario-Antonio	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

Reliability evaluation

On

BD03 for silicon line change

General Information	
Product Lines	BD03
Product Description	Power BIPOLAR
Commercial Product	TIP105
Product Group	IMS – APM
Product division	Power Bipolar
Package	TO-220
Silicon Process technology	PLANAR PNP

Locations	
Wafer fab	*Ang Mo Kio (SINGAPORE)*
Assembly plant	*SHENZHEN (China)* *LONGGANG (China)*
Reliability Lab	*IMS-APM Catania Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	June-2009	6	G.Montalto	G.Falcone	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of new silicon line BD03 for silicon line change on TIP105 device.

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

PNP Planar power transistors

4.2 Construction note

D.U.T.: TIP105 LINE: BD03

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR PNP
Die finishing back side	Au/Cr/Ni/Au
Die size	2490 x 2220 um^2
Metal 1	Al/Si
Passivation type	P-Vapox

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (SINGAPORE)*
Test program	WPIS

Assembly information	
Assembly site	SHENZHEN, LONGGANG
Package description	TO-220
Molding compound	Epoxy resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	95.5%(Pb) / 2%(Sn) / 2.5%(Ag)
Wire bonding process	Ultrasonic
Wires bonding materials/diameters	Al/Mg Base / 7 mils Al Emitter / 10 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	SHENZHEN, LONGGANG
Tester	IP test

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	TO-220	BD03	Power BIPOLAR

5.2 Reliability test plan and results summary

D.U.T.: TIP105 LINE: BD03

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTSL	N	JESD22 A-103	Ta = 150℃	77	1000H	0/77
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=48V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=50V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
AC	N	JESD22 A-102	Pa=2Atm / Ta=121℃	77	96 H	0/77

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF Thermal Fatigue	This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress).	The purpose of this test is to detect assembly defects: improper die-attach, bonding weakness and thermal mismatch among various components of the package.

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