PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-MHD/10/4730
Notification Date 01/26/2010

Qualification of ASE Weihai (China) new subcontractor for products packaged in TO92 Halogen Free

Table 1. Change Implementation Schedule

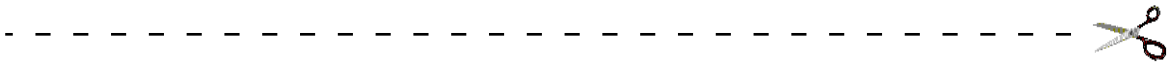
Forecasted implementation date for change	19-Jan-2010
Forecasted availabillity date of samples for customer	19-Jan-2010
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	19-Jan-2010
Estimated date of changed product first shipment	27-Apr-2010

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	All products assembled in TO92
Type of change	Package assembly location change
Reason for change	Production rationalization
Description of the change	Qualification of halogen free material set for TO92 package produced in ASE Weihai (China).
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Marking on package: last 2 digits will become "GE" instead of "9Y".
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM-MHD/10/4730**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 01/26/2010**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Gilot, Yves	Division Marketing Manager
Kaire, Jean-Claude	Division Product Manager
Paccard, Francoise	Division Q.A. Manager

Reliability and Qualification Report

Halogen free TO92 packaged in ASE Weihai (China)

PCN APM-MHD/10/4730

General Information	
Product Line	*B831/0431*
Commercial product	*TS831-5IZ-AP, TL431CZ*
Product Description	*Supervisor, Voltage reference*
Product Group	*APM*
Product division	*Standard Ic's*
Package	*TO92*
Silicon Process technology	*Hf2CMOS, Bipolar*

Locations	
Wafer fab	*Ang Mo Kio (Singapore)*
Assembly plant	*ASE Weihai*
Final Test plant	*ASE Weihai*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	23-Sept-2008	5	JM Bugnard	F Paccard	First issue

1 RELIABILITY AND QUALIFICATION EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on B831 and 0431 test vehicles to qualify halogen free material set for package TO92 produced in ASE Weihai.

1.2 Conclusion

All results are inside ST specification and TO92 with halogen free material set below described in ASE Weihai is qualified for AMPS BU.

2 DEVICES TRACABILITY

2.1 Devices description

B831: The TS831 is an ultra low power integrated circuit incorporating a high stability band-gap voltage reference and a comparator with an open drain output.
The threshold voltage is set at 4.33V for TS831-5, 4.5V for TS831-4 and 2.71V for TS831-3 by internal thermally matched resistors. The comparator exhibits a 20µs response (with 10mV overdrive) and has an open drain output active when input voltage is lower than the threshold. An internal hysteresis, 100mV for TS831-4 / TS831-5 and 60mV for TS831-3, increases the comparator's noise margin and prevents false reset operation.

0431: The TL431 is a programmable shunt voltage reference with guaranteed temperature stability over the entire operating temperature range. The output voltage may be set to any value between 2.5 V and 36 V with two external resistors.
The TL431 operates with a wide current range from 1 to 100 mA with a typical dynamic impedance of 0.22 ohm.

2.2 Wafer fabrication information

TV	B831	0431	
Wafer fabrication location	AMK6	AMK6	
Technology	HF2CMOS	Bipolar	
Die size (µm)	1.50x134mm	1.22x0.90mm	
Passivation type	Nitride+Pvapox	Nitride	

2.3 Assembly information

TV	B831	0431
Assembly site	ASE Weihai	ASE Weihai
Package description	TO92	TO92
Molding compound	KCC KTMC 1050GD	
Frame material	copper	
Die attach process	Epoxy glue	
Die attach material	amicon c990j ablestick	
Wires material & diameter	1mil	
Lead finishing	Sn	

3 RELIABILITY TESTS RESULTS

3.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	HF2CMOS/TO92	B831	
2	Bipolar/TO92	0431	
3			

Detailed results in below chapter will refer to P/N and Lot #.

3.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 2	Lot 4		
Die Oriented Tests									
HTB	N	JESD22 A-108	Tj = 125℃, BIAS	156	168 H	0/78	0/78		
					500 H	0/78	0/78		
					1000 H	0/78	0/78		
Package Oriented Tests									
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	156	168 H	0/78	0/78		
					240 H	0/78	0/78		
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃	156	100 cy	0/78	0/78		
					200 cy	0/78	0/78		
					500 cy	0/78	0/78		
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, BIAS	78	168 H	0/78			
					500 H	0/78			
					1000 H	0/78			
Other Tests									
WBS	N	AECQ100-001		30	N/A	X			See preliminary result from assy report in chapter 6
WBP	N	MILSTD883 Method 2011		30	N/A	X			
SD		JESD22 B102		20	N/A	X			

4 ANNEXES

4.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		

5 GLOSSARY

ESD	Electro Static Discharge
ELFR	Early Life Failure Rate
GL	Gate Leakage
HTB	High Temperature Bias
HTRB	High Temperature Reverse Bias
HTS	High Temperature Storage
T.H.B.	Temperature Humidity Bias
T.C.	Thermal Cycle
P.P.	Pressure Pot
P.C.	Preconditioning

6 CONSTRUCTION ANALYSIS

WBS (Wire Bond Shear):

4.7 BALL SHEAR TEST

Lower Spec Limit (LSL)	Min 21 gr	Performed by	Hongyu.Sun
Equipment	Gauge	Method	Manual
Equipment Model	400	Wire Diameter	1.0 mil

BALL SHEAR TEST	Unit									
	1	2	3	4	5	6	7	8	9	10
n1	48.29	59.6	56.54	48.54	53.91	55.95	54.58	53.45	47.19	56.96
n2	50.89	47.91	44.66	51.91	52.16	48.31	47.51	58.15	55.08	53.89
n3	52.5	53.09	52.79	52.59	51.23	48.49	52.27	50.78	49.96	54.72
Mean	50.6	53.5	51.3	51.0	52.4	50.9	51.5	54.1	50.7	55.2
Max	52.5	59.6	56.54	52.59	53.91	55.95	54.58	58.15	55.08	56.96
Min	48.29	47.91	44.66	48.54	51.23	48.31	47.51	50.78	47.19	53.89
n	3	3	3	3	3	3	3	3	3	3
Range	4.21	11.69	11.88	4.05	2.68	7.64	7.07	7.37	7.89	3.07
Std. Dev.	2.12	5.86	6.07	2.17	1.36	4.36	3.61	3.73	4.00	1.59
Ppk	4.64	1.85	1.66	4.61	7.70	2.29	2.82	2.96	2.48	7.18
SHEAR MODE :										
Al	0	0	0	0	0	0	0	0	0	0
Ball	2	2	2	2	2	2	2	2	2	2
Cratering	0	0	0	0	0	0	0	0	0	0

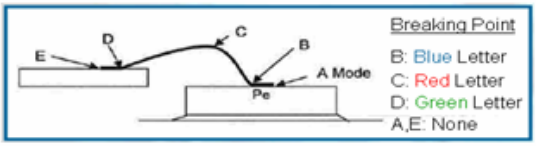
Overall Mean based on total n balls	52.1
Overall Max based on total n balls	59.6
Overall Min based on total n balls	44.66
Overall Std Dev based on total n balls	3.54
Overall Ppk based on total n balls	2.93

WBP (Wire bond Pull)

Lower Spec Limit (LSL)	Min 4.0 gr	Performed by	Hongyu.Sun
Equipment	Gauge	Method	Manual
Equipment Model	400	Wire Diameter	1.0 mil

WIRE PULL TEST	Unit									
	1	2	3	4	5	6	7	8	9	10
n1	9.80	10.24	10.38	8.75	10.23	10.08	10.25	10.03	7.93	10.15
n2	11.75	8.84	9.45	11.16	11.47	11.16	9.75	10.88	10.15	10.00
n3	10.82	10.56	10.46	9.49	10.12	10.68	11.69	9.64	11.11	10.56
Mean	10.8	9.9	10.1	9.8	10.6	10.6	10.6	10.2	9.7	10.2
Max	11.748	10.559	10.459	11.156	11.473	11.159	11.694	10.877	11.114	10.56
Min	9.804	8.844	9.451	8.747	10.118	10.084	9.75	9.636	7.93	9.997
n	3	3	3	3	3	3	3	3	3	3
Range	1.944	1.715	1.008	2.409	1.355	1.075	1.944	1.241	3.184	0.563
Std Dev	0.97	0.91	0.56	1.23	0.75	0.54	1.01	0.63	1.63	0.29
Ppk	2.02	1.82	3.09	1.32	2.53	3.55	1.87	2.78	0.99	6.12
BREAK MODE	B	B	B	B	B	B	B	B	B	B
	D	B	B	D	B	B	B	B	B	B
	B	B	B	B	B	B	D	B	D	B

Overall Mean based on total n wires	10.25
Overall Max based on total n wires	11.75
Overall Min based on total n wires	7.93
Overall Std Dev based on total n wires	0.86
Overall Ppk based on total n wires	2.44



Failure mode -

B	Failure at Ball Bond Heel
D	Failure at Stitch Bond Heel
C	Lifted Ball Bond at Die
E	Lifted Stitch Bond at frame
A	Wire Break at points other than Ball / Stitch heel

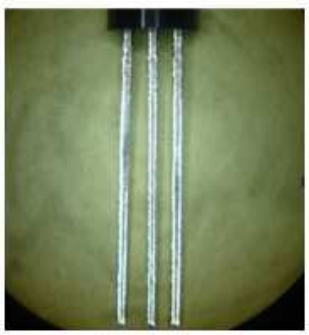
SD (Solderability)

SOLDERABILITY TEST

Upper Spec Limit (USL)	100% coverage	Performed by	Xiumei.Tian
Equipment	Solder Ability Tester	Method (i)	Dry Air Bake
Equipment Model		Method (ii)	Steam Age

Result :	Unit									
	1	2	3	4	5	6	7	8	9	10
Dry Air Bake	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Steam Age	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

REMARKS: We didn't find any reject .



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