



# PRODUCT/PROCESS CHANGE NOTIFICATION

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PCN MMS-MMY/09/4680  
Notification Date 06/17/2009

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**M24512, 512Kbit Serial I2C Bus EEPROM Redesign and  
Upgrade to the CMOSF8H Process Technology**

**Table 1. Change Implementation Schedule**

Forecasted implementation date for change	10-Jun-2009
Forecasted availability date of samples for customer	10-Jun-2009
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	10-Jun-2009
Estimated date of changed product first shipment	16-Sep-2009

**Table 2. Change Identification**

Product Identification (Product Family/Commercial Product)	M24512 products family
Type of change	Waferfab technology change
Reason for change	Line up to state of art of design
Description of the change	Redesign and Upgrade to the new CMOSF8H Process Technology
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process Techno identifier is "K" for CMOSF8H upgraded version
Manufacturing Location(s)	

**Table 3. List of Attachments**

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN MMS-MMY/09/4680
Please sign and return to STMicroelectronics Sales Office		Notification Date 06/17/2009
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved  <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark ..... ..... ..... ..... ..... ..... ..... ..... ..... .....		

## DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Division Marketing Manager
Rodrigues, Benoit	Division Product Manager
Malbranche, Jean-Luc	Division Q.A. Manager



## **M24512, 512Kbit Serial I<sup>2</sup>C Bus EEPROM Redesign and Upgrade to the CMOSF8H Process Technology**

### **What is the change?**

The **M24512**, 512Kbit Serial I<sup>2</sup>C Bus EEPROM product family, currently produced using the CMOSF8L Process Technology in the ST Rousset (France) 8 inch wafer diffusion plant has been **redesigned** and will be **upgraded** to the **CMOSF8H** Process Technology in the same wafer diffusion plant.

The same part number will support operation with bus frequency at 1 MHz, 400kHz or 100 kHz (see datasheet rev.14 dated June 2009) removing the need for M24512-H ordering when 1 MHz operation is requested (see appendix B).

Following parameters are updated:

- tCLQV = 100ns (AC characteristics at 1 MHz, 400kHz or 100 kHz)
- tNS = 80ns (AC characteristics at 1 MHz, 400kHz or 100 kHz)
- ESD HBM passes 3000V

For other parameters, upgraded version is functionally backward compatible to previous version, as per datasheet rev.13 dated Jan. 2009.

### **Why?**

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24512 in the new CMOSF8H Process Technology will increase the production capacity throughput and consequently improve the service to our customers.

Also, the new die is fitting the MLP 2x3 package (M24512-RMB6TG).

### **When?**

The production of the upgraded M24512 with the new CMOSF8H will ramp up from June 2009 and shipments can start from September 2009 onward (or earlier upon customer approval).

### **How will the change be qualified?**

The new version of the M24512 has been qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

The CMOSF8H is already qualified on the M95512 product family.

The **Qualification Report QREE0806** is available and included inside this document.

### **What is the impact of the change?**

- **Form:** marking change (see **Device marking** paragraph)
- **Fit:** no change
- **Function:** change on **AC performances** and **ESD HBM** (Datasheet updated)

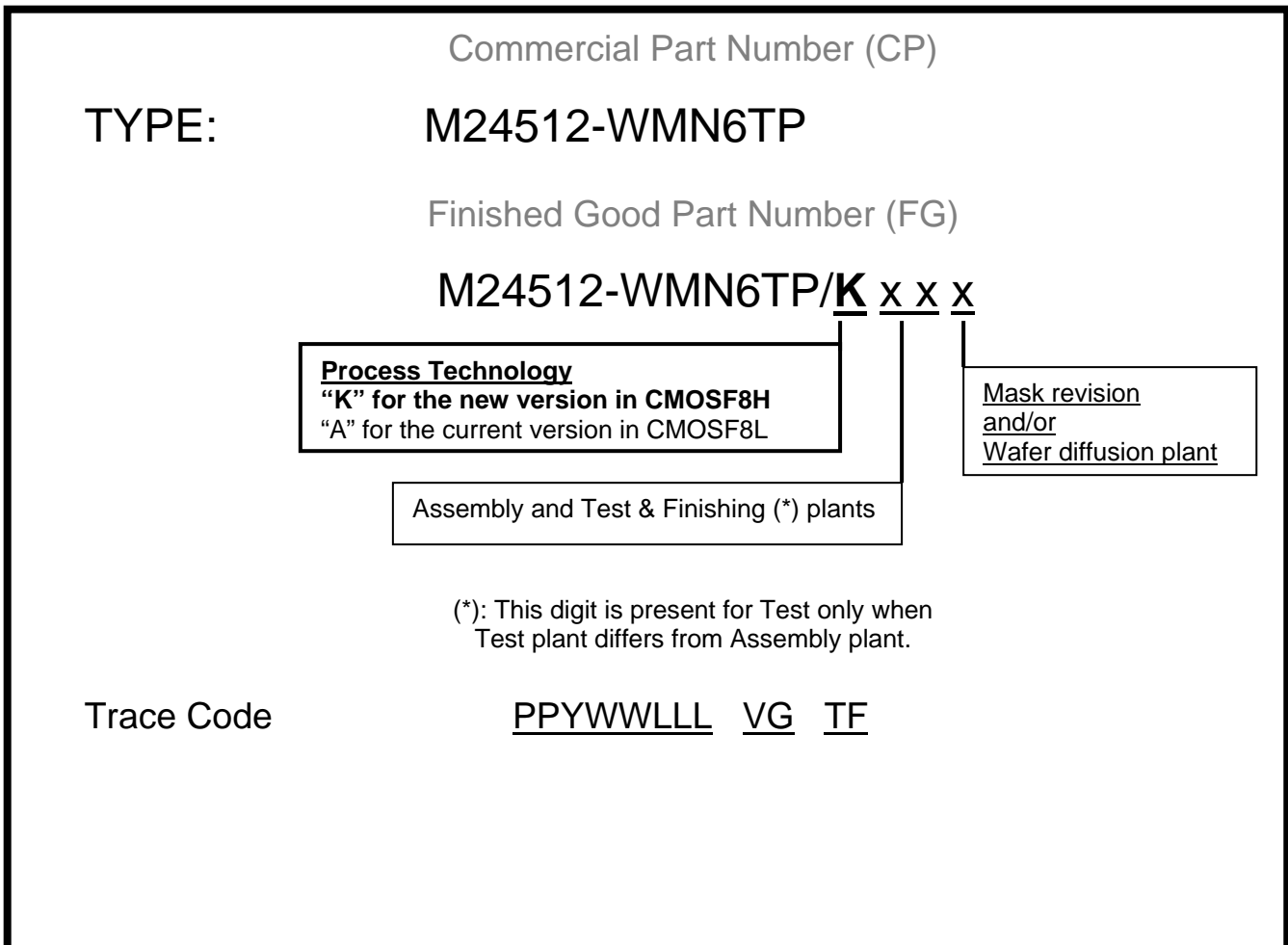
## How can the change be seen?

### - BOX LABEL MARKING

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **Process Technology** identifier is “**K**” for the **upgraded version**, this identifier being “**A**” for the current version.

→ Example for M24512-WMN6TP (2.5V to 5.5V Vcc range, SO8N – ECOPACK<sup>®</sup> 2\* compliant package)


\* ECOPACK<sup>®</sup> 2: New grade introduced to identify commonly called “Halogen-Free” products on the market. This grade is also RoHS compliant. (ECOPACK<sup>®</sup> is a registered trademark of STMicroelectronics)





## How can the change be seen?

### - DEVICE MARKING



On the DEVICE MARKING of the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit “T” for **Process Technology** identifier is “K” for the **upgraded version** in **CMOSF8H**, the identifier being “B” for the current version in CMOSF8L.

	<b>Upgraded M24512 in CMOSF8H</b>	<b>Current M24512 in CMOSF8L</b>
<b>SO8N</b> Example: M24512-WMN6TP	24512WP  PYWWK	24512WP  PYWWB

For **TSSOP8**, the difference is visible inside the product name: **upgraded version** in **CMOSF8H** is ending by “K”, the current version was ending by “P”.

	<b>Upgraded M24512 in CMOSF8H</b>	<b>Current M24512 in CMOSF8L</b>
<b>TSSOP8</b> Example: M24512-WDW6TP	412WK  PYWW	412WP  PYWW

For **SO8W**, the difference is visible inside the trace code: **upgraded version** in **CMOSF8H** is ending by “K”, the current version was ending by “B”.

	<b>Upgraded M24512 in CMOSF8H</b>	<b>Current M24512 in CMOSF8L</b>
<b>SO8W</b> Example: M24512-WMW6TG	24512WG PPLLL WX COO YWWK  e4	24512WG PPLLL WX COO YWWB  e4

P or PP= Assembly plant / country  
 LLL= chronological sequence  
 WX= wafer fab  
 COO= Country Of origin  
 Y = Last digit of the Year of Assembly  
 WW = Assembly Week code  
**T = Process Technology code/ Wafer Fab ID**

**Appendix A- Product Change Information**

<b>Product family / Commercial products:</b>	M24512 products family
<b>Customer(s):</b>	All
<b>Type of change:</b>	Wafer fab Process Technology change
<b>Reason for the change:</b>	Line up to state of art of design.
<b>Description of the change:</b>	Redesign and Upgrade to the new CMOSF8H Process Technology.
<b>Forecast date of the change:</b>	Week 24 / 2009
<b>Forecast date of <u>Qualification samples</u> availability for customer(s):</b>	Available
<b>Forecast date for the internal STMicroelectronics change, <u>Qualification Report</u> availability:</b>	QREE0806 is available and included inside this document
<b>Marking to identify the changed product:</b>	Process and fab ID see marking above
<b>Description of the qualification program:</b>	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
<b>Product Line(s) and/or Part Number(s):</b>	See Appendix B
<b>Manufacturing location:</b>	Rousset 8 inch wafer fab
<b>Estimated date of first shipment:</b>	Week 38 / 2009



**Appendix B: Concerned Commercial Part Numbers:**

<b>M24512-WMN6P</b>		
<b>M24512-WMN6TP</b>		
<b>M24512-WDW6TP</b>		
<b>M24512-WMW6G</b>		
<b>M24512-WMW6TG</b>		
<b>M24512-RDW6TP</b>		
<b>M24512-RMN6P</b>		
<b>M24512-RMN6TP</b>		
<b>M24512-HRDW6TP</b>	replaced by	M24512-RDW6TP
<b>M24512-HRMN6P</b>	replaced by	M24512-RMN6P
<b>M24512-HRMN6TP</b>	replaced by	M24512-RMN6TP

**Appendix C: Qualification Report:**



**QREE0806  
Qualification report**

New design / M24512-W, M24512-R, M24512-DR  
using the CMOSF8H technology in the Rousset 8" Fab

Table 1. Product information

General information	
Commercial product	M24512-RMN6P M24512-RMN6TP M24512-WMN6P M24512-WMN6TP M24512-RDW6TP M24512-WDW6TP
Product description	512 Kbit serial I <sup>2</sup> C bus EEPROM with three Chip Enable lines
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8", France
Electrical Wafer Sort test plant location	ST Rousset, France

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Amkor P1, Philippines	Amkor P3, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Amkor P1, Philippines	Amkor P3, Philippines

Reliability / Qualification assessment: PASS

## 1 Reliability evaluation overview

### 1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new M24512-W, M24512-R and M24512-DR devices using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M24512-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M24512-R and M24512-DR devices

The CMOSF8H is a new advanced silicon process technology in the ST Rousset 8" fab, with Double Poly and Double Metal process. This document serves for the qualification of the named product and the named silicon process technology in the named diffusion fab.

### 1.2 Conclusion

The new M24512-W, M24512-R and M24512-DR devices using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab have passed the reliability requirements and all products described in [Table 1](#) are qualified.

Refer to [Section 3: Reliability test results](#) for details on the reliability test results.

## 2 Device characteristics

### Device description

The M24512-W, M24512-R, M24512-DR devices are I<sup>2</sup>C-compatible electrically erasable programmable memories (EEPROM). They are organized as 64 Kb × 8 bits.

I<sup>2</sup>C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I<sup>2</sup>C bus definition.

The device behaves as a slave in the I<sup>2</sup>C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Refer to the product datasheet for more details.

### 3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in [Table 3](#).

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24512 <sup>(1)</sup>	CMOSF8H	ST Rousset 8"	CDIP8	Engi assy <sup>(2)</sup>
M95512	CMOSF8H	ST Rousset 8"	CDIP8	Engi assy <sup>(2)</sup>

- Die-oriented reliability tests mainly based on M95512 product (same silicon process technology, same design core between 512 Kbit I<sup>2</sup>C and 512 Kbit SPI / Metal mask option for bus control).
- CDIP8 is a ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicle and silicon process technologies used for package qualification are presented in [Table 4](#).

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95512 <sup>(1)</sup>	CMOSF8H	ST Rousset 8"	SO8N	ST Shenzhen & Amkor P1
			TSSOP8	ST Shenzhen & Amkor P1
			UFDFPN8 (MLP8) 2 x 3 mm	Amkor P3
M24512	CMOSF8H	ST Rousset 8"	SO8W	Amkor P1
			WLCSP	Stats ChipPac

- Package qualification results of M95512 are applicable (same silicon process technology, same memory array between 512 Kbit I<sup>2</sup>C and 512 Kbit SPI / Metal mask option for bus control).

#### 3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- In [Table 5](#) for die-oriented tests
- In [Table 6](#) for SO8N ST Shenzhen & Amkor P1 package-oriented tests
- In [Table 7](#) for TSSOP8 ST Shenzhen & Amkor P1 package-oriented tests
- Reliability tests on all other packages are planned, but results are not yet available.

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Reliability test results

**Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)<sup>(1)</sup>**

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95512			M24512 <sup>(2)</sup>
						Lot 1	Lot 2	Lot 3	Lot 4
EDR	High temperature operating life after endurance								
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	-
EDR	Data retention after endurance								
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTSL at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	-
LTOL	Low temperature operating life								
	JESD22-A108	-40 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	-
HTSL	High temperature storage life								
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80	0/80	0/80	-
WEB	Program/erase endurance cycling + bake								
	Internal spec.	1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	1 Million cycles / 48 hrs	0/80 <sup>(3)</sup>	0/80 <sup>(3)</sup>	0/80 <sup>(3)</sup>	-
ESD HBM	Electrostatic discharge (human body model)								
	AEC-Q100-002 JESD22-A114	C = 100 pF, R = 1500 Ω	27	1	N/A	Pass > 3000 V	Pass > 3000 V	Pass > 3000 V	Pass > 3000 V
ESD MM	Electrostatic discharge (machine model)								
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	6	1	N/A	Pass > 300 V	Pass > 300 V	Pass > 300 V	Pass > 300 V
LU	Latch-up (current injection and overvoltage stress)								
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	1	N/A	Class II Level A	Class II Level A	Class II Level A	Class II Level A

1. See Table 8: List of terms for a definition of abbreviations.
2. Die-oriented reliability tests mainly based on M95512 product (same silicon process technology, same design core between 512 Kbit I<sup>2</sup>C and 512 Kbit SPI / Metal mask option for bus control).
3. First rejects after 3 million cycles + bake.



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Reliability test results

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**Table 6. Package-oriented reliability test plan and result summary (SO8N / Shenzhen & Amkor P1)<sup>(1)</sup>**

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95512 <sup>(2)</sup>			M24512
Lot1	Lot2	Lot3	Lot 4						
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/400	0/400	0/400	-
THB <sup>(3)</sup>	Temperature humidity bias								
	AEC-Q100- JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	1	1008 hrs	0/80	0/80	0/80	-
TC <sup>(3)</sup>	Temperature cycling								
	AEC-Q100- JESD22-A104	-65 °C / +150 °C	80	1	1000 cycles	0/80	0/80	0/80	-
TMSK <sup>(3)</sup>	Thermal shocks								
	JESD22-A106	-55 °C / +125 °C	25	1	200 shocks	0/80	0/80	0/80	-
AC <sup>(3)</sup>	Autoclave (pressure pot)								
	AEC-Q100- JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80	0/80	0/80	-
HTSL <sup>(3)</sup>	High temperature storage life								
	AEC-Q100- JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	-
ELFR	Early life failure rate								
	AEC-Q100- 008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100- JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See [Table 8: List of terms](#) for a definition of abbreviations.

2. Package qualification results of M95512 are applicable (same silicon process technology, same memory array between 512 Kbit I<sup>2</sup>C and 512 Kbit SPI / Metal mask option for bus control).

3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

**M24512, 512Kbit Serial I<sup>2</sup>C Bus EEPROM  
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Reliability test results

**Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / Shenzhen & Amkor P1)<sup>(1)</sup>**

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95512 <sup>(2)</sup>			M24512
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/400	0/400	0/400	-
THB <sup>(3)</sup>	Temperature humidity bias								
	AEC-Q100- JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	1	1008 hrs	0/80	0/80	0/80	-
TC <sup>(3)</sup>	Temperature cycling								
	AEC-Q100- JESD22-A104	-65 °C / +150 °C	80	1	1000 cycles	0/80	0/80	0/80	-
TMSK <sup>(3)</sup>	Thermal shocks								
	JESD22-A106	-55 °C / +125 °C	25	1	200 shocks	0/80	0/80	0/80	-
AC <sup>(3)</sup>	Autoclave (pressure pot)								
	AEC-Q100- JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80	0/80	0/80	-
HTSL <sup>(3)</sup>	High temperature storage life								
	AEC-Q100- JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	-
ELFR	Early life failure rate								
	AEC-Q100- 008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100- JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See [Table 8: List of terms](#) for a definition of abbreviations.
2. Package qualification results of M95512 are applicable (same silicon process technology, same memory array between 512 Kbit I<sup>2</sup>C and 512 Kbit SPI / Metal mask option for bus control).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.



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## 4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

## 5 Glossary

Table 8. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

## 6 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Jun-2009	1	Initial release.

**M24512, 512Kbit Serial I<sup>2</sup>C Bus EEPROM  
Redesign and Upgrade to the CMOSF8H Process Technology**

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<b>Document Revision History</b>		
Date	Rev.	Description of the Revision
June 03, 2009	1.00	First draft creation

<b>Source Documents &amp; Reference Documents</b>		
Source document Title	Rev.:	Date:

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