



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN HED-AUD/09/4677
Notification Date 06/15/2009

**L165V; L165H; TDA2006V; TDA2006H; TDA2030V; TDA2030H;
TDA2030AV; TDA2030AH TRANSFER FROM AMK5 (5" wafers) TO AMK6 (6" wafers)**

Table 1. Change Implementation Schedule

Forecasted implementation date for change	08-Jun-2009
Forecasted availability date of samples for customer	08-Jun-2009
Forecasted date for STMicroelectronics change Qualification Plan results availability	08-Jun-2009
Estimated date of changed product first shipment	22-Jun-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	L165 line
Type of change	Waferfab location change
Reason for change	capacity rationalization
Description of the change	As part of the running program to convert to 6" wafers the silicon lines diffused on the bipolar processes, the products L165V; L165H; TDA2006V; TDA2006H; TDA2030V; TDA2030H; TDA2030AV; TDA2030AH, diffused on LAAT process, will be transferred from Ang Mo Kio 5" production line to Ang Mo Kio 6" production line. SCHEDULE SUBJECT TO CUSTOMER APPROVAL
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	traceability code "V6" for AMK6 fab
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Angelici, Marco	Division Marketing Manager
Onetti, Andrea Mario	Division Product Manager
Piccoli, Massimo	Division Q.A. Manager



**L165V; L165H; TDA2006V; TDA2006H;
TDA2030V; TDA2030H; TDA2030AV;
TDA2030AH TRANSFER FROM AMK5 (5”
wafers) TO AMK6 (6” wafers)**

WHAT

As part of the running program to convert to 6” wafers the silicon lines diffused on the bipolar processes, the products L165V; L165H; TDA2006V; TDA2006H; TDA2030V; TDA2030H; TDA2030AV; TDA2030AH, diffused on LAAT process, will be transferred from Ang Mo Kio 5” production line to Ang Mo Kio 6” production line.

WHY

To rationalize the production capacity.

HOW

The bipolar LAAT diffusion process family is qualified and running in volumes since 2003.

The qualification will be done through test vehicles belonging to the same LAAT process family (namely L203 ; L613 ; LX05).

Here following the Reliability Reports.



RELIABILITY EVALUATION on L203 LAAT process Ang-Mo-Kio 6”

Abstract

The L203 diffused in Ang-Mo-Kio 6” have been positively evaluated from the Reliability point of view. A HTRB test has been performed on one lot.

Conclusion

The results obtained in the stress test performed, as shown in detail at page 2, point out that the diffusion wafer change from 5” to 6” in Ang-Mo-Kio of LAAT process does not generate any weakness on L203 device from the reliability viewpoint.



Reliability test conditions and results

N	TEST NAME	Device	CONDITIONS [SPEC]	SAMPLE SIZE x Lot	DEFECTS*	NOTES
1	HTRB	L203	Vs=50V, Tj=150°C, 1000h	50 pcs	0	-

* Defect is any device rejected at the readout electrical testing or failing additional acceptance criteria according to the specified procedure.

Device construction note:

DIE FEATURES	
Die Code	: L203CA6
Diffusion process	: LAAT
Wafer diameter	: 6"
Diffusion site	: Ang-Mo-Kio
Die size	: 2.34 x 1.3 mm ²
Metal level	: 1, Al
Passivation	: Nitride
Back finishing	: Cr/Ni/Au
Diffusion lot	: 6240L5F

PACKAGE FEATURES	
Technical code	: AB17*L203CA6
Package name	: PDIP 16L 0.25
Assembly site	: MUAR
Die attach	: Ablebond 8390
Wire Bonding	: Au, 1.3 mils
Moulding compound	: HYSOL MG46F

Attachments:

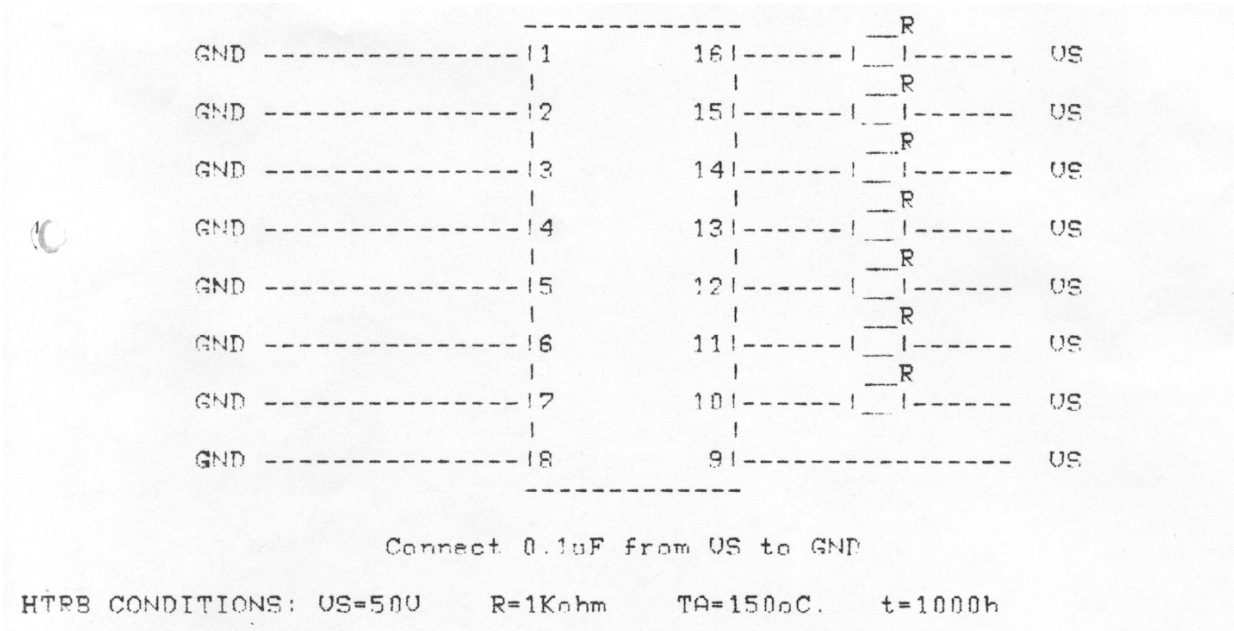
- 1) Reliability tests description
- 2) Electrical stress tests schematics and pin configuration

ATTACHMENT 1: RELIABILITY TEST DESCRIPTION

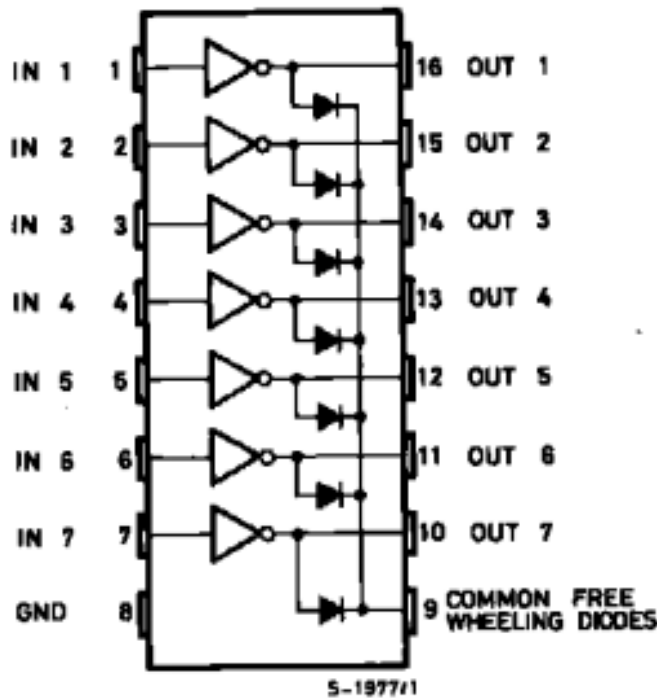
TEST NAME	DESCRIPTION	PURPOSE
HTRB: High Temperature Reverse Bias Test	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: -) low power dissipation; -) max. supply voltage compatible with diffusion process and internal circuitry limitations; -) max. junction temperature.	To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.

ATTACHEMENT 2:

HTRB DIAGRAM



PIN CONFIGURATION





RELIABILITY EVALUATION on L613 LAAT process Ang-Mo-Kio 6”

Abstract

The L613 diffused in Ang-Mo-Kio 6” have been positively evaluated from the Reliability point of view. A HTRB test has been performed on one lot.

Conclusion

The results obtained in the stress test performed, as shown in detail at page 2, point out that the diffusion wafer change from 5” to 6” in Ang-Mo-Kio of LAAT process does not generate any weakness on L613 device from the reliability viewpoint.



Reliability test conditions and results

N	TEST NAME	Device	CONDITIONS [SPEC]	SAMPLE SIZE x Lot	DEFECTS*	NOTES
1	HTRB	L613	Vs=50V, Tj=150°C, 1000h	50 pcs	0	-

* Defect is any device rejected at the readout electrical testing or failing additional acceptance criteria according to the specified procedure.

Device construction note:

DIE FEATURES	
Die Code	: L613AA6
Diffusion process	: LAAT
Wafer diameter	: 6"
Diffusion site	: Ang-Mo-Kio
Die size	: 2.64 x 1.35 mm ²
Metal level	: 1, Al
Passivation	: Nitride
Back finishing	: Cr/Ni/Au
Diffusion lot	: 6240L5F

PACKAGE FEATURES	
Technical code	: ACC7*L613AA6
Package name	: PDIP 18L 0.25
Assembly site	: MUAR
Die attach	: Ablebond 8390
Wire Bonding	: Au, 1 mil
Moulding compound	: Nitto MP180

Attachments:

- 1) Reliability tests description
- 2) Electrical stress tests schematics and pin configuration

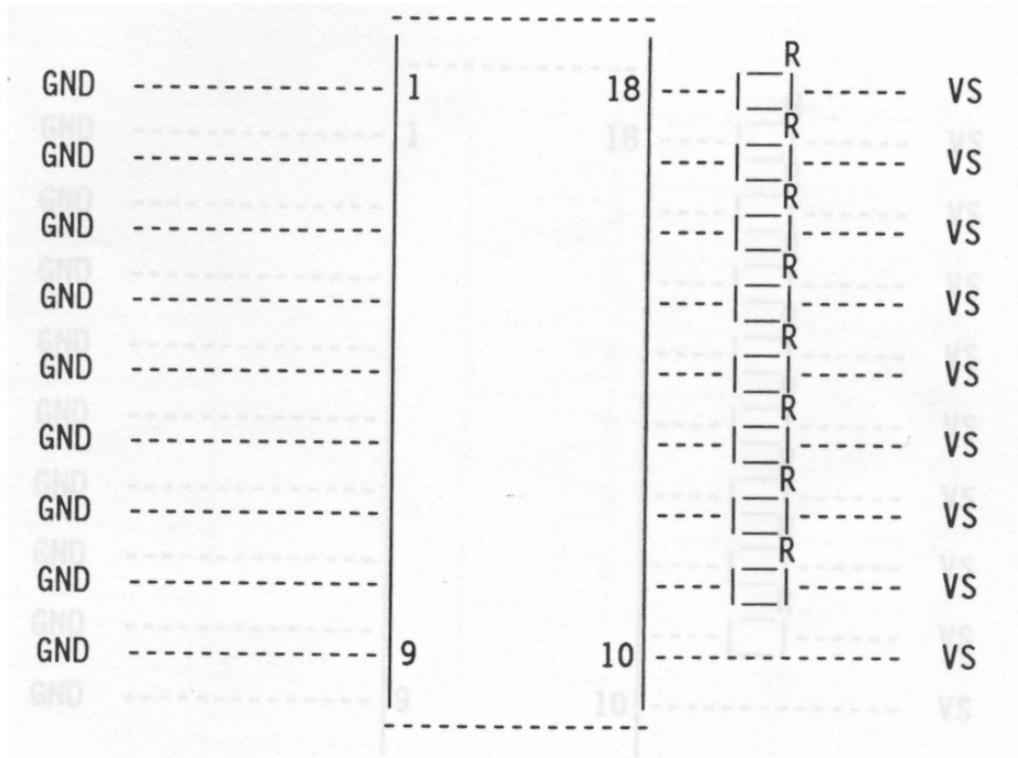
ATTACHMENT 1: RELIABILITY TEST DESCRIPTION

TEST NAME	DESCRIPTION	PURPOSE
HTRB: High Temperature Reverse Bias Test	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: -) low power dissipation; -) max. supply voltage compatible with diffusion process and internal circuitry limitations; -) max. junction temperature.	To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.



ATTACHEMENT 2:

HTRB DIAGRAM



R= 1Kohm

PIN CONFIGURATION

IPIN	DESCRIPTION	IPIN	DESCRIPTION
1	INPUT 1	10	COMMON DIODES
2	INPUT 2	11	IOUTPUT 8
3	INPUT 3	12	IOUTPUT 7
4	INPUT 4	13	IOUTPUT 6
5	INPUT 5	14	IOUTPUT 5
6	INPUT 6	15	IOUTPUT 4
7	INPUT 7	16	IOUTPUT 3
8	INPUT 8	17	IOUTPUT 2
9	IGND	18	IOUTPUT 1



RELIABILITY EVALUATION PLAN AND RESULTS
ON L7805 – LAAT180 TECHNOLOGY

REL-6333-173/077.03W
Line: LX05 (EW2)

Date: 26/08/2003
Package: TO220

TEST	TEST DESCRIPTION	STM TEST CONDITIONS	STM S.S.	RESULTS Fail/s.s.	GENERIC DATA
HTB	High Temperature Bias	TA=125°C - BIAS=35V TIME=1000 HOURS	77	0/77	0/385 (*)
THB	Temperature Humidity Bias	TA=85°C - RH=85% - BIAS=24V TIME=1000HOURS	77	0/77	0/385 (*)
PPT	Pressure Pot	TA=121°C -PA=2ATM TIME=240HOURS	77	0/77	0/385 (*)
TCT	Temperature Cycles AIR TO AIR	TA=-65°C TO 150°C 1 HOUR / CYCLE TIME=1000CYCLES	77	0/77	0/385 (*)
HTS	High Temperature Storage	TA=150°C	77		0/385 (*)
ENV. SEQ	Environmental Sequence	TC=100CY + PPT=168H	50		0/250 (*)
TH. SH.	Thermal Shocks	TA=-65°C TO 150°C 10min / CYCLES (LIQUID TO LIQUID)	77	0/77	0/385 (*)
TFT	THERMAL FATIGUE	$\Delta t= 105^{\circ}\text{C}$	77		0/385 (*)

- (*) Generic data for all year 2003

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