PRODUCT/PROCESS CHANGE NOTIFICATION

PCN HED-AUD/09/4606
Notification Date 05/22/2009

STA013$ ASSEMBLY PLANT CHANGE FROM AMKOR ATP1 PHILIPPINES TO STM MUAR

Table 1. Change Implementation Schedule

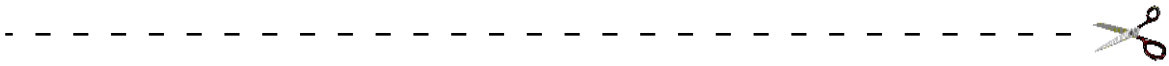
Forecasted implementation date for change	15-May-2009
Forecasted availabillity date of samples for customer	15-May-2009
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-May-2009
Estimated date of changed product first shipment	21-Aug-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	STA013$; STA013$13TR
Type of change	Multiple types of changes
Reason for change	Production capacity and bill of materials for assembly rationalization
Description of the change	STM is going to change the back end plant of STA013$ from AMKOR ATP1 Philippines (subcontractor) to ST MUAR (Malaysia) On the same time: The molding compound will be changed from NITTO GC7450KS2 to SUMITOMO EME7026 . The glue for die attach will be changed from ABLESTICK 8290 to HITACHI EN4900 ST12. The leadframe will be changed from post-plated to pre-plated.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Traceability code: "99" for Muar assembly
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN HED-AUD/09/4606**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 05/22/2009**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Angelici, Marco	Division Marketing Manager
Onetti, Andrea Mario	Division Product Manager
Piccoli, Massimo	Division Q.A. Manager

STA013$ ASSEMBLY PLANT CHANGE FROM AMKOR ATP1 PHILIPPINES TO STM MUAR

WHAT

STM is going to change the back end plant of STA013$ from AMKOR ATP1 Philippines (subcontractor) to ST MUAR (Malaysia)
On the same time:
The molding compound will be changed from NITTO GC7450KS2 to SUMITOMO EME7026 .
The glue for die attach will be changed from ABLESTICK 8290 to HITACHI EN4900 ST12.
The leadframe will be changed from post-plated to pre-plated.

WHY

To rationalize production capacity as already done for similar products in the same package, using the same Bill Of Materials.

HOW

SO is a package family already qualified and in mass production on MUAR plant with assembly process using the same materials as STA013$.
In particular V421 is belonging to the same family (SO24 package: same package family and materials; same HCMOS6 Front End technology).
Following the reliability reports.

Reliability Report

Assembly site transfer, molding compound change, glue for die attach change, leadframe change

General Information	
Product Line	*V071 CAL*
Product Description	*MPEG LAYER III DECODER*
Finished Good Code	*STA013*
Product division	*AUDIO*
Package	*SO 28*
Silicon process technology	*HCMOS6*

Locations	
Wafer fab location	*UMC8C*
Assembly plant location	MUAR
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	May, 13, 2009		Fabio Fiabane	

Issued by **Fabio Fiabane**

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the reliability evaluation performed on V071 CAL.

V071 CAL is processed in *HCMOS6* diffused in *UMC8C* and assembled in *SO 28* in *ST MUAR.*

1.2 Conclusion

Taking in account that:

- V071 CAL die is qualified,
- SO28 package is qualified,
- V071 CAL follows the qualification of the test vehicle V421 BAL (RR001809CS2047),
- The workability of V071 CAL in SO28 package gave positive results,

we can conclude that *V071 CAL* device, processed in HCMOS6 in UMC8C and assembled in SO28 in Muar, can be released to production from a reliability point of view.

2 DEVICE CHARACTERISTICS

2.1 Device description

2.1.1 Generalities

STA013
STA013B STA013T

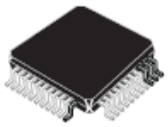
MPEG 2.5 LAYER III AUDIO DECODER

- SINGLE CHIP MPEG2 LAYER 3 DECODER SUPPORTING:
  - All features specified for Layer III in ISO/IEC 11172-3 (MPEG 1 Audio)
  - All features specified for Layer III in ISO/IEC 13818-3.2 (MPEG 2 Audio)
  - Lower sampling frequencies syntax extension, (not specified by ISO) called MPEG 2.5
- DECODES LAYER III STEREO CHANNELS, DUAL CHANNEL, SINGLE CHANNEL (MONO)
- SUPPORTING ALL THE MPEG 1 & 2 SAMPLING FREQUENCIES AND THE EXTENSION TO MPEG 2.5:
  48, 44.1, 32, 24, 22.05, 16, 12, 11. 025, 8 KHz
- ACCEPTS MPEG 2.5 LAYER III ELEMENTARY COMPRESSED BITSTREAM WITH DATA RATE FROM 8 Kbit/s UP TO 320 Kbit/s
- DIGITAL VOLUME CONTROL
- DIGITAL BASS & TREBLE CONTROL
- SERIAL BITSTREAM INPUT INTERFACE
- ANCILLARY DATA EXTRACTION VIA I2C INTERFACE.
- SERIAL PCM OUTPUT INTERFACE (I^2S AND OTHER FORMATS)
- PLL FOR INTERNAL CLOCK AND FOR OUTPUT PCM CLOCK GENERATION
- LOW POWER CONSUMPTION:
  85mW AT 2.4V
- CRC CHECK AND SYNCHRONISATION ERROR DETECTION WITH SOFTWARE INDICATORS
- I^2C CONTROL BUS
- LOW POWER 3.3V CMOS TECHNOLOGY
- 10 MHz, 14.31818 MHz, OR 14.7456 MHz EXTERNAL INPUT CLOCK OR BUILT-IN INDUSTRY STANDARD XTAL OSCILLATOR DIFFERENT FREQUENCIES MAY BE SUPPORTED UPON REQUEST TO STM

APPLICATIONS

- PC SOUND CARDS
- MULTIMEDIA PLAYERS

SO28



TQFP44

LFBGA64

ORDERING NUMBERS: STA013$ (SO28)
STA013T$ (TQFP44)
STA013B$ (LFBGA 8x8)

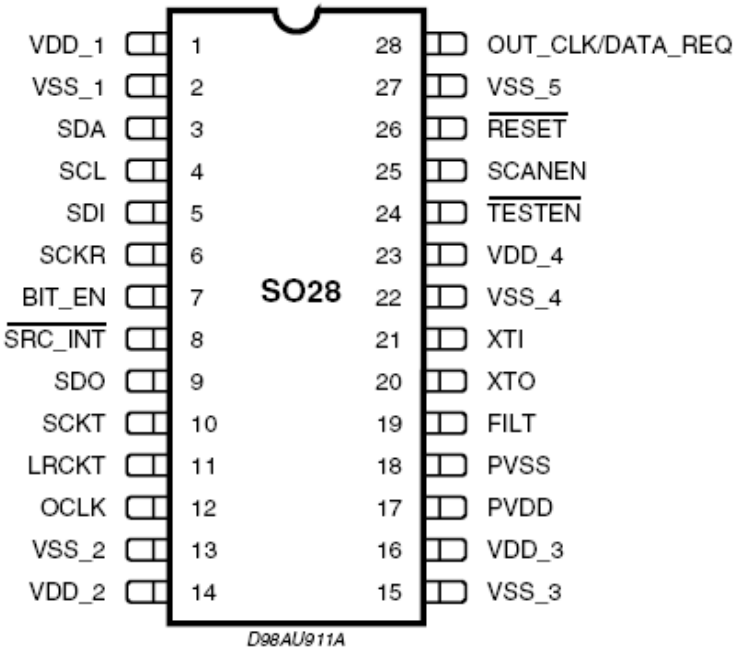
DESCRIPTION

The STA013 is a fully integrated high flexibility MPEG Layer III Audio Decoder, capable of decoding Layer III compressed elementary streams, as specified in MPEG 1 and MPEG 2 ISO standards. The device decodes also elementary streams compressed by using low sampling rates, as specified by MPEG 2.5.

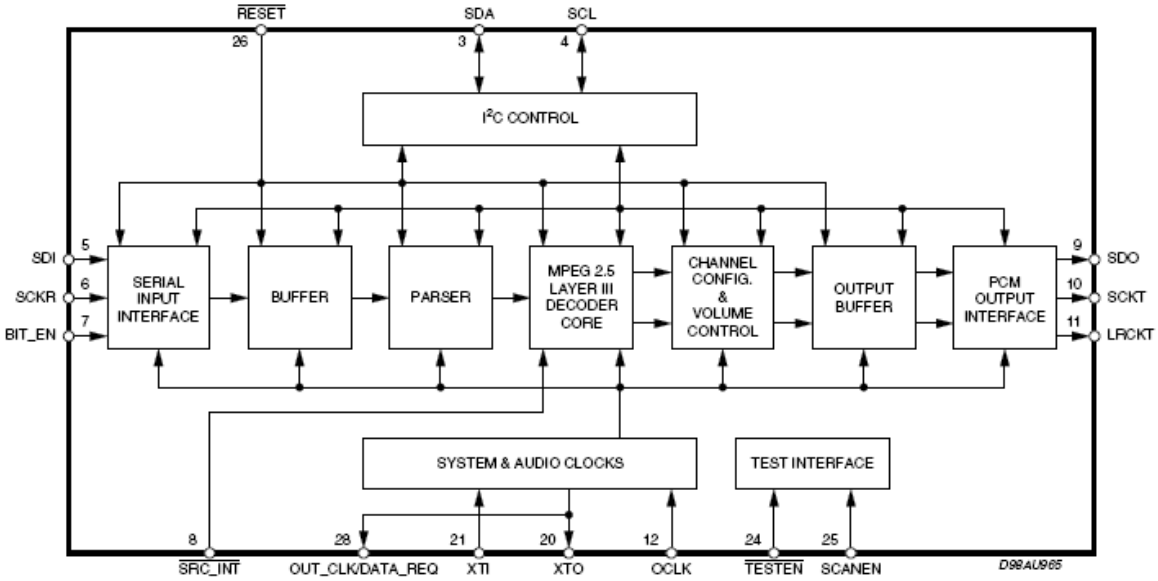
STA013 receives the input data through a Serial Input Interface. The decoded signal is a stereo, mono, or dual channel digital output that can be sent directly to a D/A converter, by the PCM Output Interface. This interface is software programmable to adapt the STA013 digital output to the most common DACs architectures used on the market.

The functional STA013 chip partitioning is described in Fig.1.

2.1.2 Pin connection



2.1.3 Block diagram

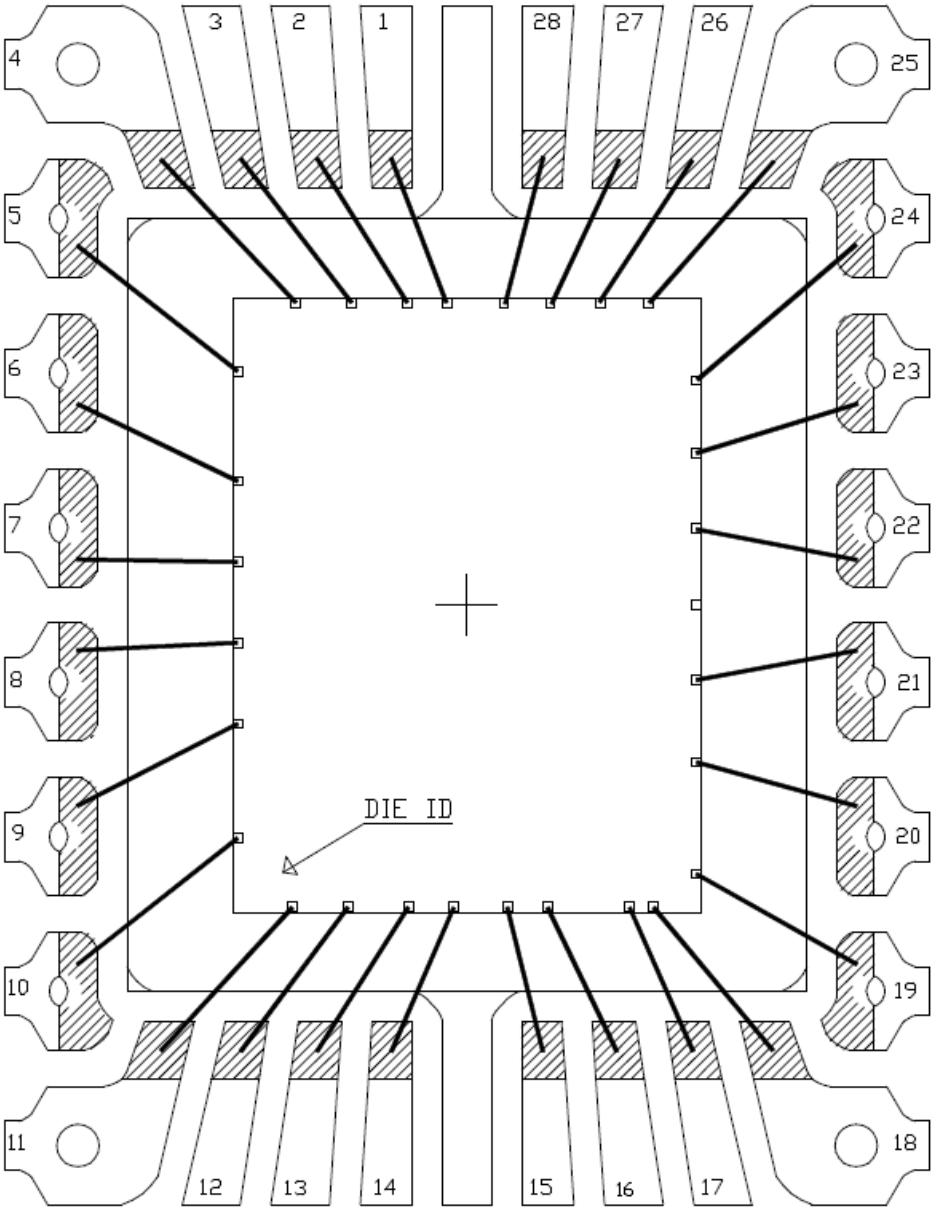


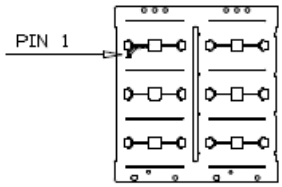
2.1.4 Bonding diagram

BONDING DIAGRAM FOR LINE : V071 PACKAGE : L R

FRAME PAD : .220 x .250 inch / 5,588 x 6,350 mm DIE SIZE : inch

Dimensions in the bsa





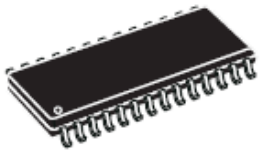
SOP 28L

BLANK BOND. DIAG. REF. : 0078705

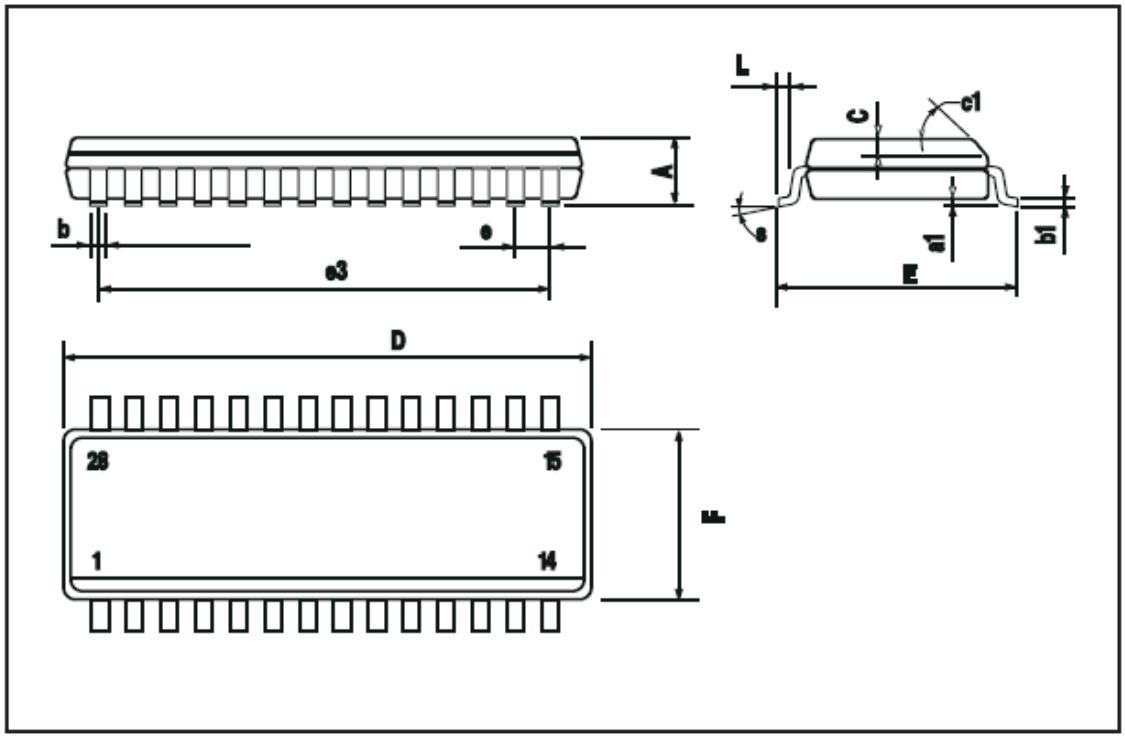
2.1.5 Package outline/Mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO28



2.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*UMC/USC; SUBCO 8`*
Wafer diameter	*8*
Silicon process technology	*HCMOS6*
Die size	*5270 x 4070 micron*

Assembly Information	
Assembly plant location	*MUAR B/E*
Package description	*SO 28*
Die pad size	*5.5 x 6.3 mm*
Molding compound	*SUMITOMO*
Wires bonding materials/diameters	*Au D1.2*
Die attach material	*HITACHI*

Reliability Report

General Information	
Product Line	*V421 BAL*
Product Description	*MICRO CONTROLLER ASIC*
Product division	*I&PC*
Package	*SO24*
Silicon process technology	*HCMOS6*

Locations	
Wafer fab location	*UMC8C*
Assembly plant location	*MUAR*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	27-Feb-09	10	M. Benzoni	Original document

Issued by

Massimo Benzoni

Reviewed by

Alceo Paratore

Approved by

Antonino Motta

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
SOP 2.6.10	: General product qualification procedure
SOP 2.6.11	: Program management fro product qualification
SOP 2.6.12	: Design criteria for product qualification
SOP 2.6.14	: Reliability requirements for product qualification
SOP 2.6.19	: Process maturity level
SOP 2.6.2	: Process qualification and transfer management
SOP 2.6.20	: New process / New product qualification
SOP 2.6.7	: Product maturity level
SOP 2.6.9	: Package and process maturity management in Back End
SOP 2.7.5	: Automotive products definition and status

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of V421 BAL device diffused in UMC8C and assembled in SO24 in MUAR.

Considering that the V421 AAP diffused in PHOENIX is already qualified (see report RR35.04.CS2039), below is the list of the trials performed:

Die Oriented Tests

- High temperature Operating Life

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the trials performed **the V421 BAL diffused in UMC8C and assembled in SO24 in MUAR can be qualified from reliability viewpoint.**

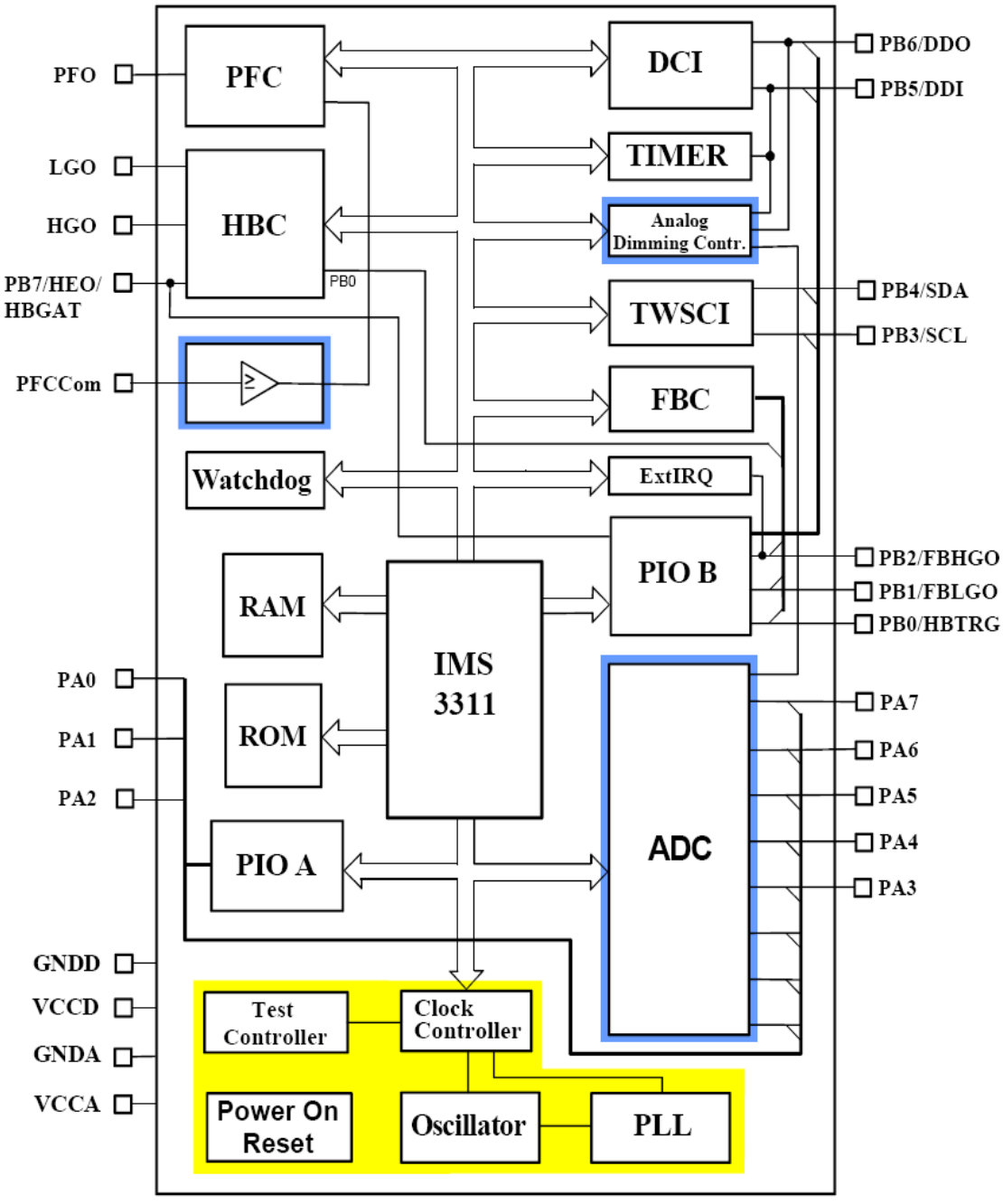
3 DEVICE CHARACTERISTICS

3.1 Device description

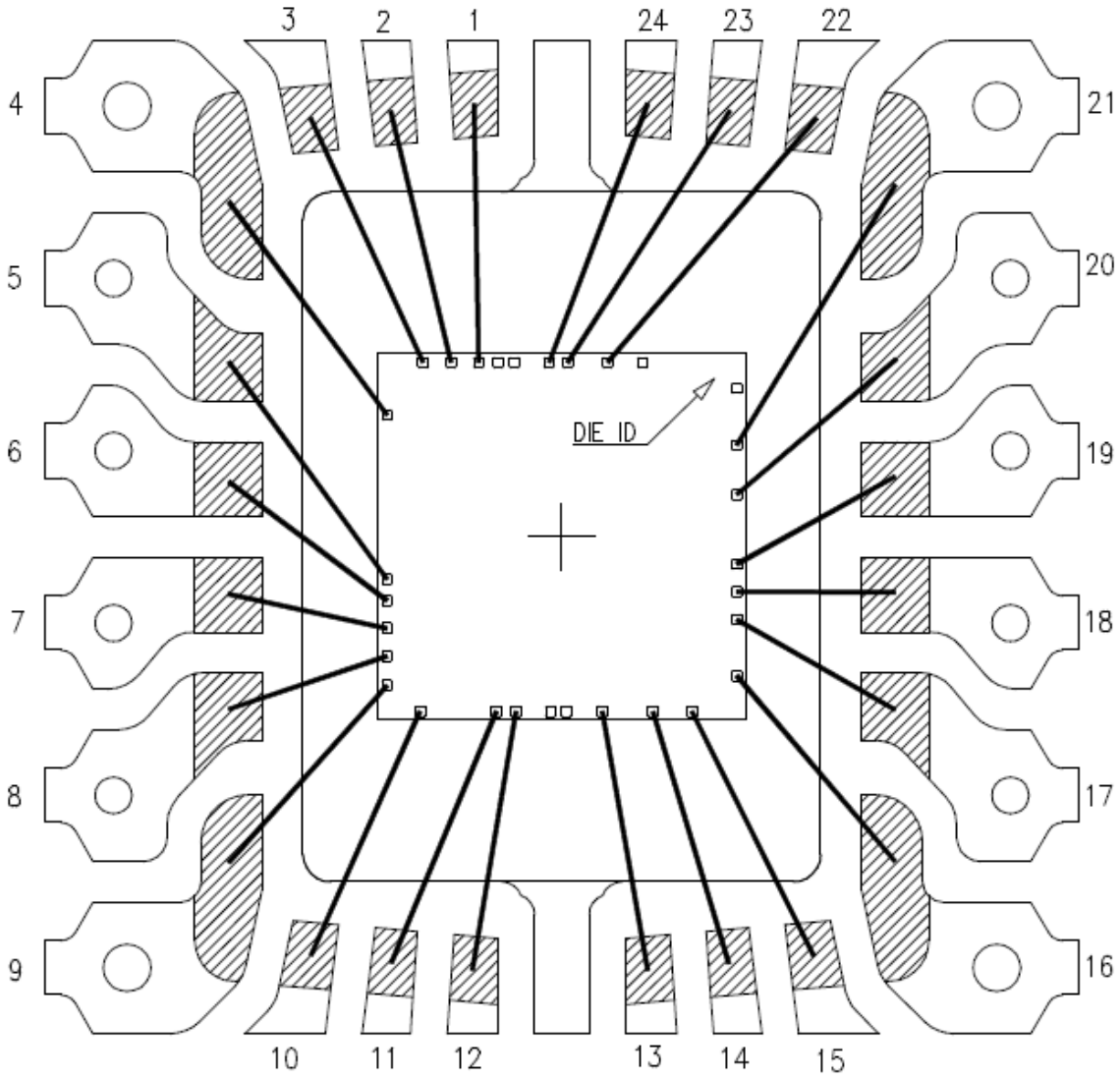
3.1.1 Pin connection

Pin Number	Symbol	Pin Number	Symbol
1	PFO	13	PA3
2	LGO	14	PA4
3	HGO	15	PA5
4	HEO/HBGAT/PB7	16	PA6
5	PFCCom	17	PA7
6	PA0	18	HBTRG/PB0
7	PA1	19	FBLGO/PB1
8	PA2	20	FBHGO/PB2
9	GNDD	21	SCL/PB3
10	VCCD	22	SDA/PB4
11	GNDA	23	DDI/PB5
12	VCCA	24	DDO/PB6

3.1.2 Block diagram

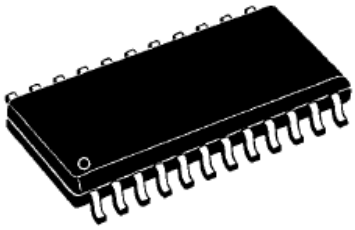


3.1.3 Bonding diagram

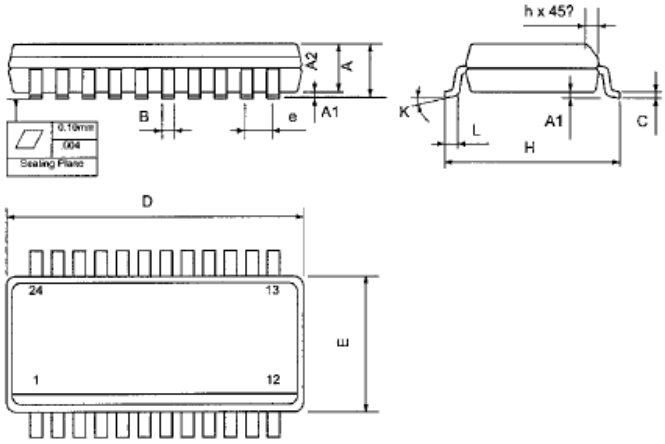


3.1.4 Package outline/Mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2			2.55			0.100
B	0.33		0.51	0.013		0.0200
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0,050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
k	0° (min.), 8° (max.)					
L	0.40		1.27	0.016		0.050



Clear marking of Pin 1 required



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*UMC8C*
Wafer diameter	*8 inches*
Wafer thickness	*375 µm*
Silicon process technology	*HCMOS6*
Die finishing back side	*Raw Silicon*
Die size	*2910x2900 µm*
Bond pad metallization layers	*AlCu*
Passivation	*PSG + SiN*
Metal levels	*5*

Assembly Information	
Assembly plant location	*MUAR*
Package description	*SO24*
Die pad size	*3.810x5.080 mm*
Molding compound	*SUMITOMO EME7026*
Wires bonding materials/diameters	*Au / 1.2mils*
Die attach material	*HITACHI EN4900*
Lead solder material	*NiPdAu*

4 TESTS RESULTS SUMMARY

4.1 Test plan and results summary

Die Oriented Tests						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results Fail/SS**
HTOL	High Temperature Operating Life					
	PC before	**Tj=150℃ VCCA=VCCD=3.6V**	**77**	3	**1000h**	**0/231**

Package Oriented Tests						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results Fail/SS**
PC	Pre-Conditioning: Moisture sensitivity level 3					
		192h 30℃/60% - 3 reflow PBT 260℃	**154**	1		**0/154**
		192h 30℃/60% - 3 reflow PBT 260℃	**77**	3		**0/231**
AC	Autoclave					
	PC before	**121℃ 2atm**	**77**	1	**168h**	**0/77**
TC	Temperature Cycling					
	PC before	**Temp. range: -50/+150℃**	**77**	1	**1000cy**	**0/77**
HTSL	High Temperature Storage					
	No bias	**Tamb=150℃**	**77**	1	**1000h**	**0/77**

Electrical Characterization Tests						
Test	**Method**	**Conditions**	**Sample/ Lots**	**Number of lots**	**Duration**	**Results Fail/SS**
ESD	Electro Static Discharge					
	Human Body Model	**+/- 2kV**	**3**	1		**0/3**
	Charge Device Model	**+/- 750V (*)**	**3**	1		**0/3**
		+/- 500V	**3**	1		**0/3**
LU	Latch-Up					
	Over-voltage and Current Injection	**Tamb=85℃ Jedec78 – Level B**	**3**	1		**0/3**

(*) Only Corner Pin

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25℃.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25℃.

TEST CONDITIONS:

- Ta= -50℃ to +150℃(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25℃.
- Final Testing (168hrs) @ Ta=25℃.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121℃
- test time= 168 hrs

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-100mA	Inom+100mA	VCCA, VCCD=5.4V
IN high: 3.6V	-100mA	Inom+100mA	VCCA, VCCD=5.4V

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25℃
- ESD discharging @ Ta=25℃
- Final Testing @ Ta=25℃

TEST CONDITIONS:

- **Human Body Model** JEDEC STANDARD JESD22-A114
  CDF-AEC-Q100-002
- **Charge Device Model** JEDEC STANDARD JESD22-C101
  CDF-AEC-Q100-011

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