PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-PMT/09/4520
Notification Date 04/23/2009

Die bonding process change from Solder Paste to Power Glue for Package: SO-8

Table 1. Change Implementation Schedule

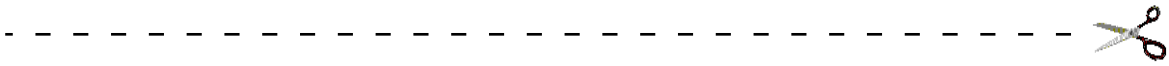
Forecasted implementation date for change	16-Apr-2009
Forecasted availabillity date of samples for customer	16-Apr-2009
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	16-Apr-2009
Estimated date of changed product first shipment	23-Jul-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly material change
Reason for change	Assembly process optimization and simplified flow.
Description of the change	We are going to change the preform compound in the die bonding process (named also die attach), from Solder Paste to Power Glue to selected devices in SO-8 package, manufactured in Bouskoura (MOROCCO). The Power Glue QMI9507-2A05 ha shown better electrical performances and improving of assembly yield compare to the Solder Paste compound Pb/Sn/Ag.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Week code: 29/2009
Manufacturing Location(s)	1]St Bouskoura 2 - Morocco

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM-PMT/09/4520**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 04/23/2009**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Giudice, Maurizio	Division Marketing Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

Reliability Report

Power MOSFET SO-8 Package
with
Power Glue

General Information	
Product Lines	FL6C- FL3F- 333A
Product Description	Power MOSFET
Commercial Products	STS5DNF60L- STS12NF30L- STS8C5H30L
Product Group	IMS - APM
Product division	Power MOSFET
Package	SO-8
Silicon Process technology	STripFET™ Power MOSFET

Locations	
Wafer fab	*Ang Mo Kio (SINGAPORE)* *CT6 Catania (ITALY)* *M5 Catania (ITALY))*
Assembly plant	*BOUSKOURA (MOROCCO)*
Reliability Lab	*IMS-APM Catania Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	April-2009	10	G.Montalto	G.Falcone	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualifications of the new die attach material (Power Glue).

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STS5DNF60L LINE: FL6C PACKAGE: SO-8

Wafer/Die fab. information	
Wafer fab manufacturing location	*CT6 Catania*
Technology	*StripFET II Enhancement N- channel Power MOSFET*
Die finishing back side	Ti/Ni/Au
Die size	1720 x 2500 µm^2
Metal	Al/Si
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Catania*
Test program	WPIS

Assembly information	
Assembly site	BOUSKOURA (MOROCCO)
Package description	SO-8
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Power Glue
Wire bonding process	Thermosonic
Wires bonding materials	Au Source Au Gate
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	BOUSKOURA (MOROCCO)
Tester	IPTEST

D.U.T.: STS12NF30L LINE: FL3F PACKAGE: SO-8

Wafer/Die fab. information	
Wafer fab manufacturing location	*CT6 Catania*
Technology	*StripFET II Enhancement N- channel Power MOSFET*
Die finishing back side	Ti/Ni/Au
Die size	2490x3880 µm^2
Metal	Al/Si
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	CATANIA
Test program	WPIS

Assembly information	
Assembly site	BOUSKOURA (MOROCCO)
Package description	SO-8
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Power Glue
Wire bonding process	Thermosonic
Wires bonding materials	Au Source Au Gate
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	BOUSKOURA (MOROCCO)
Tester	IPTEST

D.U.T.: STS8C5H30L LINE: 333A PACKAGE: SO-8

Wafer/Die fab. information	
Wafer fab manufacturing location	*M5 Catania*
Technology	*StripFET IIII Enhancement N- channel Power MOSFET*
Die finishing back side	Ti/Ni/Au
Die size	1640 x 1470 µm^2
Metal	Al/Si
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania
Test program	WPIS

Assembly information	
Assembly site	BOUSKOURA (MOROCCO)
Package description	SO-8
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Power Glue
Wire bonding process	Thermosonic
Wires bonding materials	Au Gate Au Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	BOUSKOURA (MOROCCO)
Tester	IPTEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STS5DNF60L,	FL6C	Power MOSFET
2	STS12NF30L,	FL3F	Power MOSFET
3	STS8C5H30L.	333A	Power MOSFET

5.2 Reliability test plan and results summary

D.U.T.: STS5DNF60L LINE: FL6C PACKAGE: SO-8

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 15V	77	1000H	0/77
HTSL	N	JESD22 A-103	Ta = 150℃	77	1000H	0/77
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=48V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=50V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

D.U.T.: STS12NF30L LINE: FL3F PACKAGE: SO-8

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 15V	77	1000H	0/77
HTSL	N	JESD22 A-103	Ta = 150℃	77	1000H	0/77
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=24V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=24V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

D.U.T.: STS8C5H30L LINE: 333A PACKAGE: SO-8

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 15V	77	1000H	0/77
HTSL	N	JESD22 A-103	Ta = 150℃	77	1000H	0/77
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TC	Y	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF Thermal Fatigue	This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress).	The purpose of this test is to detect assembly defects: improper die-attach, bonding weakness and thermal mismatch among various components of the package.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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