



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-AAM/09/4449
Notification Date 04/27/2009

**Transfer of HCMOSTD process logic devices from CSMC
(China) to AMK6 (ST in-house plant)**

Table 1. Change Implementation Schedule

Forecasted implementation date for change	18-Jun-2009
Forecasted availability date of samples for customer	20-Apr-2009
Forecasted date for STMicroelectronics change Qualification Plan results availability	20-Apr-2009
Estimated date of changed product first shipment	27-Jul-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab location change
Reason for change	Higher manufacturing flexibility.
Description of the change	Moving of HCMOS4 Diffusion Line from CSMC (Subcontractor in China) to STMicroelectronics in-house diffusion plant, AMK6, in Singapore.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	See "V6" as Wafer code in traceability code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN APM-AAM/09/4449
Please sign and return to STMicroelectronics Sales Office		Notification Date 04/27/2009
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark		

DOCUMENT APPROVAL

Name	Function
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Calderoni, Michele	Division Q.A. Manager

Reliability Report

On
HCMOS4 TX - AMK6- Technology
Process Qualification
Test Vehicle: 74LX1G04BJR – Flip Chip 4 Package

General Information	
Product Line	EF04 <i>The 74LX1G04 is a low voltage CMOS SINGLE INVERTER fabricated with sub-micron silicon gate and double-layer metal wiring C2MOS technology.</i>
Product Description	74LX1G04BJR <i>Advanced and Analog Logic</i>
Commercial Product	IMS - APM GROUP
Product Group	Flip Chip 4
Product Division	500UM PITCH ,300UM BALL
Package Description	HCMOS4 TX
Silicon Process Technology	

Locations	
Wafer fabrication location	Ang Mo Kio (AMK6)
Assembly plant location	UBM at AMK5, Bumping and testing at SHENZEN
Final test plant location	SHENZEN

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
0.1	October-08	7	Giovanni Presti Stefania Motta	Original document Catania Q & Reliability

Reliability is the attitude of element to satisfy required function in fixed conditions during established time.

IMS (Industrial & Multisegment Sector)
APM (Analog, Power, MEMS) Group
Voltage Regulator, Interface, Advanced logic & Power RF
Quality & Reliability

Report ID: REL6043-286W08

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

HCMOS4TX DIFFUSION TRANSFER FROM CARROLLTON 6" to AMK 6".

Aim of this report is to present the results of the reliability evaluations performed on 74LX1G04BJR device, used as test vehicle for Process qualification in order to qualify HCMOS4 TX technology diffused in AMK6.

No changes in devices design or devices layout, no changes in devices structure, no changes in back-end operations

1.2 Conclusion

The final reliability results are positive.

2 DEVICE CHARACTERISTICS

2.1 Device description

The 74LX1G04 is a low voltage CMOS SINGLE INVERTER fabricated with sub-micron silicon gate and double-layer metal wiring C2MOS technology. It is ideal for 1.65 to 5.5 VCC operations and low power and low noise applications. The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. Power down protection is provided on input and output and 0 to 7V can be accepted on inputs with no regard to the supply voltage. It can be interfaced to 5V signal environment for inputs in mixed 3.3/5V system. All inputs and outputs are equipped with protection circuits against static discharge.

2.1.1 Wafer fabrication information

- Wafer fabrication manufacturing location: AMK6
- Technology: HCMOS4 TX
- Die size: 0.9 x 0.9

2.1.2 Assembly information

- Assembly site: UBM at AMK5, Bumping and testing at SHENZHEN
- Package description: Flip Chip 4 bumps, 500um pitch, 300UM Ball

3 RELIABILITY TESTS RESULTS

3.1 Reliability test plan and results summary

Include here the tests plan and the results summary.

Die oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
HTB	High Temperature Bias				
		Ta = 125°C, Vdd = 7V	77x3 Lots	1000 h	0/231
HTS	High Temperature Storage				
		Ta = 150°C	77x3 Lots	1000 h	0/231

All samples are assembled on PCB (soldering profile according to JEDEC 020D)

Package oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
T.H.B.	Temperature Humidity Bias				
		Ta=85°C Rh=85%, Vdd= 5V	77x1 Lot	1000 h	0/77
T.C.	Thermal Cycle				
		TA=-40°C TO 125°C (1 HOUR/CYCLE)	77x1 Lot	500 cy	0/77
T.H.S.	Temperature Humidity Storage				
		TA=85°C – Rh=85%	77x1 Lot	1000 h	0/77
S.M.D.	SMD INDUCED STRESS				
		IR 3 times @ Tpeak=260°C According to JEDEC020D	154x2 Lots 231x 1 Lot	Parameter deviation within spec. limits at end of test	Parameter deviation within spec. limits after go no go test

All samples are assembled on PCB (soldering profile according to JEDEC 020D)

ESD test

Zap circuit HBM 11-C; Zap vs. VCC, Zap vs. GND, Zap vs. I/O, Zap +, Zap -

ESD Model	Stress voltage (V)	Result
HBM	2 KV	Passed

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ESD test is satisfactory.

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Latch-Up test

L/U	Stress Condition	Result
Input and Output Injection	0mA to -500mA; 5.5V	Passed
Power Supply Over Voltage	Input set to VCC; Input set to GND	Passed

Latch-up tests are satisfactory.

3.2 Die oriented tests

These tests are performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and reverse biased.

The purpose of this test is to detect surface defects such as poor passivation, presence of contaminants, metal corrosion, etc

3.3 Package oriented tests

These tests are performed in order to check device life in various environmental conditions in an accelerated way. Detectable failure mechanisms are metal corrosion, cracking of die, and mechanical damage to the device case.

4 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
SOP 2610	: General product qualification procedure
Internal ST specification	: Reliability Tests and criteria for qualifications (CORPORATE Q&R RULES)
...	

5 GLOSSARY

HTB	High Temperature Bias (Operative Life)
HTS	High Temperature Storage
T.H.B.	Temperature Humidity Bias
T.C.	Thermal Cycle
T.H.S.	Temperature Humidity Storage
S.M.D.	Surface Mounting Device Stress
P.C.B.	Printed Circuit Board

6 ANNEXES

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