



# PRODUCT/PROCESS CHANGE NOTIFICATION

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PCN APM-SLI/09/4411  
Notification Date 03/25/2009

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**Halogen Free Resin for SOT23 and TSOT23 coming from Carsem**

**Table 1. Change Implementation Schedule**

Forecasted implementation date for change	16-Jun-2009
Forecasted availability date of samples for customer	18-Mar-2009
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	18-Mar-2009
Estimated date of changed product first shipment	24-Jun-2009

**Table 2. Change Identification**

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly material change
Reason for change	Extension of ECOPACK Program to "Halogen Free"
Description of the change	The change described in this document is the introduction of a new Halogen Free molding compound, the Hitachi CEL9220HF13, which will be used from wk 20 2009 onwards, in the production of SOT23 and TSOT23 packages at the Carsem plant in Malaysia. This change does not impact the electrical, dimensional and thermal parameters of the products, so the information currently published in the relevant datasheets will remain unchanged. There are also no changes in the packing modes and the standard delivery quantities. All test results required to qualify the CEL9220HF13 resin, are included in the attached qualification report
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	The new product will be identified by the "ECOPACK 2" showed on the box label
Manufacturing Location(s)	

**Table 3. List of Attachments**

Customer Part numbers list	
Qualification Plan results	

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Customer Acknowledgement of Receipt		PCN APM-SLI/09/4411
Please sign and return to STMicroelectronics Sales Office		Notification Date 03/25/2009
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved  <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark ..... ..... ..... ..... ..... ..... ..... ..... .....		

## DOCUMENT APPROVAL

Name	Function
Riviera, Antonio	Division Marketing Manager
Naso, Lorenzo	Division Product Manager
Calderoni, Michele	Division Q.A. Manager



## Reliability Report

*Halogen Free Resin for SOT23 - Carsem  
Hitachi CEL9220HF13*

General Information		Locations	
Product Line	KR33 <i>Ultra low drop voltage regulators with inhibit low ESR output capacitors compatible</i>	Wafer fab	AMK 6"
Product Description		Assembly plant	Carsem
P/N	LD2981CM33	Reliability Lab	IMS-APM Catania Reliability Lab.
Product Group	Voltage Regulator		
Product division	Voltage Regulator & Interface		
Package	SOT23		
Silicon Process technology	B120II		
Production mask set rev.	NKR0326		

### DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	July 2008	8	Alfio Rao Giuseppe Giacobello	Giovanni Presti	First issue

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## **1 APPLICABLE AND REFERENCE DOCUMENTS**

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

## **2 GLOSSARY**

DUT	Device Under Test
SS	Sample Size

## **3 RELIABILITY EVALUATION OVERVIEW**

### **3.1 Objectives**

Reliability qualification on CEL9220HF13 - halogen Free Resin for SOT23 package. Assembly location Carsem

### **3.2 Conclusion**

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



## **4 DEVICE CHARACTERISTICS**

### **4.1 Device description**

The LD2981AB/C series are 100 mA fixed-output voltage regulator. The low drop-voltage and the ultra low quiescent current make them suitable for low noise, low power applications and in battery powered systems. The quiescent current in sleep mode is less than 1  $\mu$ A when INHIBIT pin is pulled low.

### **4.2 Construction note**

P/N LD2981CM33	
<b>Wafer/Die fab. information</b>	
Wafer fab manufacturing location	AMK 6"
Technology	BI20II
Die finishing back side	Lapped Silicon
Die size	1.47*0.99mm
Passivation type	PVAPOX/NITRIDE/POLYIMIDE
<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	ASIA PAC SINGAPORE EWS
Tester	QT100
Test program	RRXXSQ**.CTS
<b>Assembly information</b>	
Assembly site	CARSEM
Package description	Sot23
Molding compound	Hitachi CEL9220HF13
Frame material	Cu+Ag spot
Die attach process	Soft solder
Die attach material	Ablestik 84-1LMISR4
Wire bonding process	Thermo sonic ball bonding
Wires bonding materials/diameters	Au - 1.0mils
Lead finishing process	Electroplating
Lead finishing/bump solder material	Pure tin
<b>Final testing information</b>	
Testing location	Carsem M
Tester	QT200
Test program	KRXFSL33.CTS





## 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicle

Lot #	Assy Lot	Process/ Package	Product Line	Comments
1	ENG2207AR	SOT23	KR33	LD2981CM33
2	ENG2207BR	SOT23	KR33	LD2981CM33
3	ENG2207CR	SOT23	KR33	LD2981CM33

Detailed results in below chapter will refer to P/N and Lot #.

### 5.2 Test plan and results summary

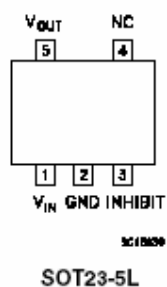
P/N LD2981CM33

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die Oriented Tests									
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	231	96 H	0/77	0/77	0/77	
					168 H	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	231	100 cy	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS= 15V	231	168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	

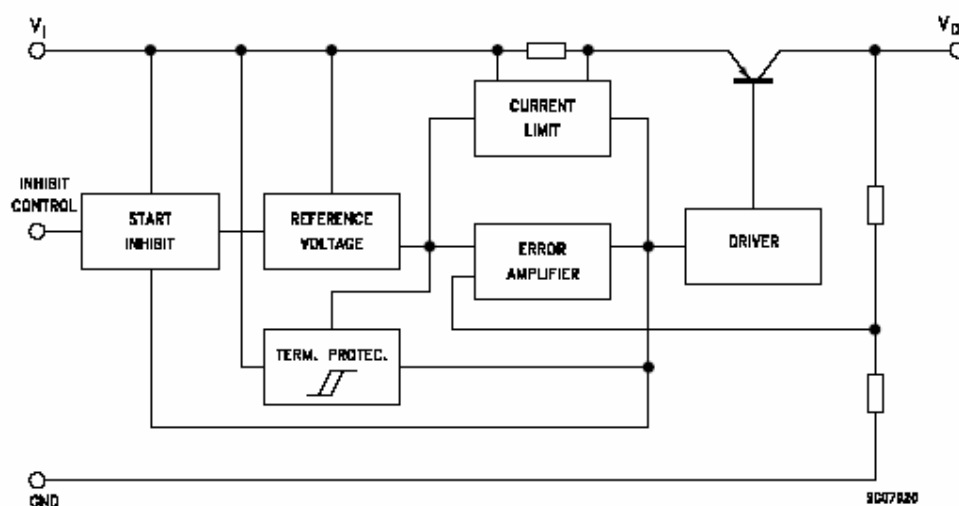
## 6 ANNEXES

### 6.1 Device details

#### 6.1.1 Pin connection

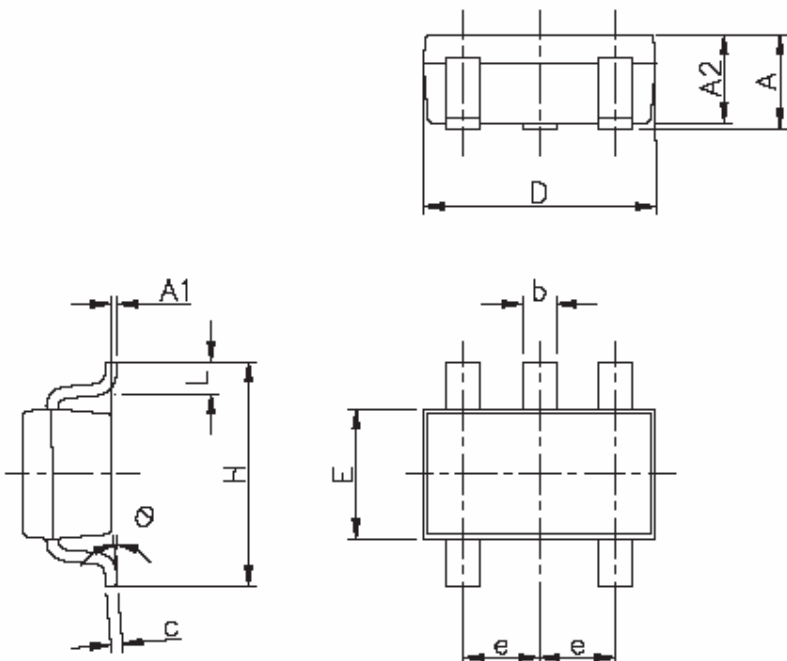


#### 6.1.2 Block diagram



### 6.1.3 Package outline/Mechanical data

SOT23-5L mechanical data						
Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6

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## 6.2 Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTSL</b> High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
<b>AC</b> Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>THB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.



## Reliability Report

### Halogen Free Resin for TSOT23 - Carsem Hitachi CEL9220HF13

General Information		Locations	
Product Line	UT92 <i>Ultra low drop-low noise</i>	Wafer fab	AGRATE 8"
Product Description	BiCMOS voltage regulators <i>low ESR capacitors</i>	Assembly plant	Carsem M
P/N	LD3985G18R <i>compatible</i>	Reliability Lab	IMS-APM Catania Reliability Lab.
Product Group	Voltage Regulator		
Product division	Voltage Regulator & Interface		
Package	TSOT23		
Silicon Process technology	BCD5		
Production mask set rev.	CUT90A		

## DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	July 2008	8	Giuseppe Giacobello Alfio Rao	Giovanni Presti	First issue

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Document reference	Short description
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## **2 GLOSSARY**

DUT	Device Under Test
SS	Sample Size

## **3 RELIABILITY EVALUATION OVERVIEW**

### **3.1 Objectives**

Reliability qualification on CEL9220HF13 - halogen Free Resin for TSOT23 package. Assembly location Carsem

### **3.2 Conclusion**

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



## **4 DEVICE CHARACTERISTICS**

### **4.1 Device description**

The LD3985xx provides up to 150 mA, from 2.5 V to 6 V input voltage. The ultra low drop-voltage, low quiescent current and low noise make it suitable for low power applications and in battery powered systems.

### **4.2 Construction note**

P/N LD3985G18R	
<b>Wafer/Die fab. information</b>	
Wafer fab manufacturing location	AGRATE 8"
Technology	BCD5
Die finishing back side	Raw Silicon
Die size	1.33*0.96mm
Passivation type	PVAPOX/NITRIDE/PIX
<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	No Test
Tester	No Test
Test program	No Test
<b>Assembly information</b>	
Assembly site	CARSEM M
Package description	TSOT23
Molding compound	Hitachi CEL9220HF13
Frame material	Cu+Ag spot
Die attach process	Soft solder
Die attach material	Ablestik 84-1LMISR4
Wire bonding process	Thermo sonic ball bonding
Wires bonding materials/diameters	Au - 1.0mils
Lead finishing process	Electroplating
Lead finishing/bump solder material	Pure tin
<b>Final testing information</b>	
Testing location	Carsem M
Tester	QT200
Test program	UTX2QT92.CTS





## 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicle

Lot #	Assy Lot	Process/ Package	Product Line	Comments
1	ENG2208AR	TSOT23	UT92	LD3985G18R
2	ENG2208BR	TSOT23	UT92	LD3985G18R
3	ENG2208CR	TSOT23	UT92	LD3985G18R

Detailed results in below chapter will refer to P/N and Lot #.

### 5.2 Test plan and results summary

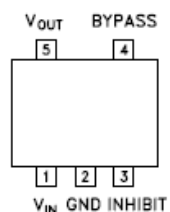
P/N LD3985G18R

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die Oriented Tests									
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	231	96 H	0/77	0/77	0/77	
					168 H	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	231	100 cy	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS=5V	231	168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	

## 6 ANNEXES

### 6.1 Device details

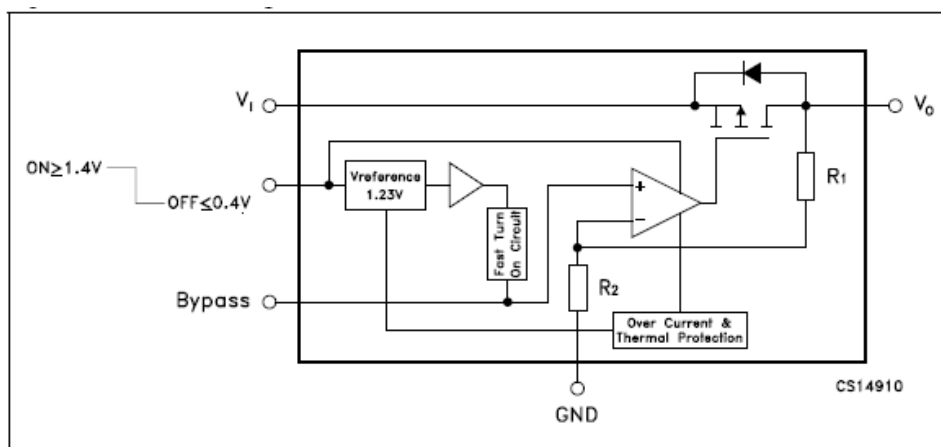
#### 6.1.1 Pin connection



CS15440

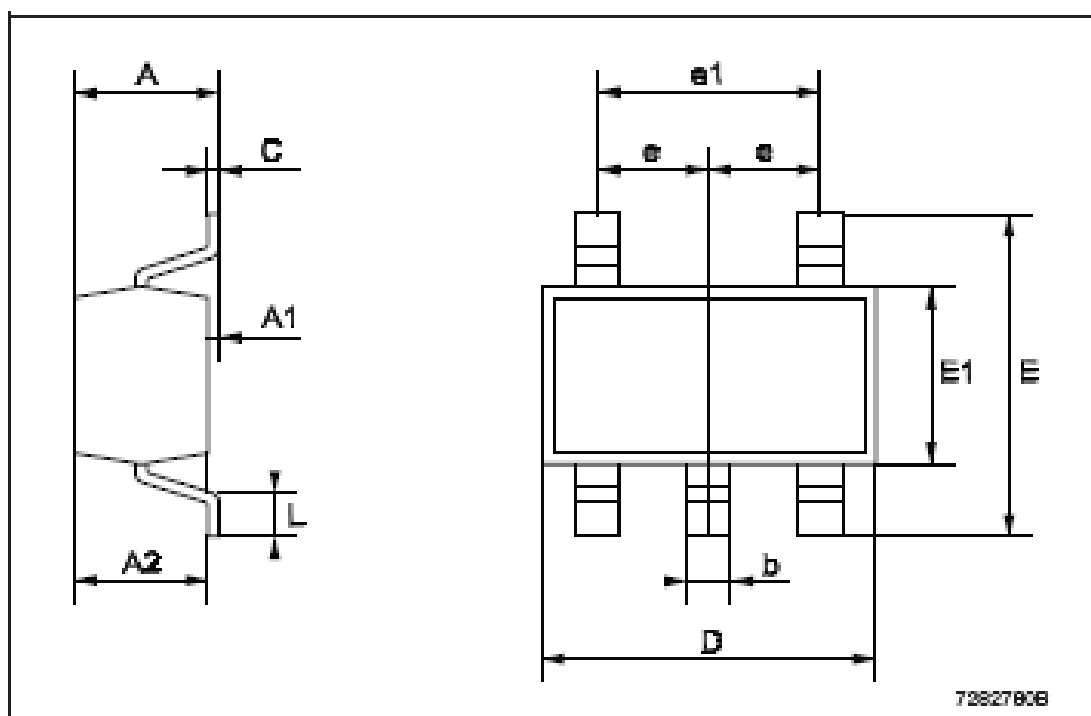
SOT23-5L/TSOT23-5L

#### 6.1.2 Block diagram



### 6.1.3 Package outline/Mechanical data

TSOT23-5L mechanical data						
Dim.	mm.			mla.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			43.3
A1	0		0.1			3.9
A2	0.7		1.0	27.8		39.4
b	0.3		0.5	11.8		19.7
C	0.08		0.2	3.1		7.9
D		2.9			114.2	
E		2.8			110.2	
E1		1.8			83.0	
e		0.95			37.4	
e1		1.9			74.8	
L	0.3		0.8	11.8		23.8





## 6.2 Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTSL</b> High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
<b>AC</b> Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>THB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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