PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM/09/4406
Notification Date 03/30/2009

DPAK Single Gauge Back-End Capacity Extension for Power MOSFET and Power Bipolar - Shenzhen (China)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	08-Jun-2009
Forecasted availabillity date of samples for customer	23-Mar-2009
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	23-Mar-2009
Estimated date of changed product first shipment	29-Jun-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly material change
Reason for change	To improve service and increase DPAK capacity
Description of the change	Following the continuous improvement of our service and in order to be ready to support the market demand of Power MOSFET and Power Bipolar, the products listed in the PCN will be also manufactured using Single Gauge frame production line. The products are in agreement with ST standards and guarantee the same quality and the same electrical characteristics as the ones assembled with Dual Gauge frame. Devices used for qualification are available as Samples.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Power MOSFET: Week code: 20/09, Power Bipolar: Letter "S" as additional info field
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	**PCN APM/09/4406**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 03/30/2009**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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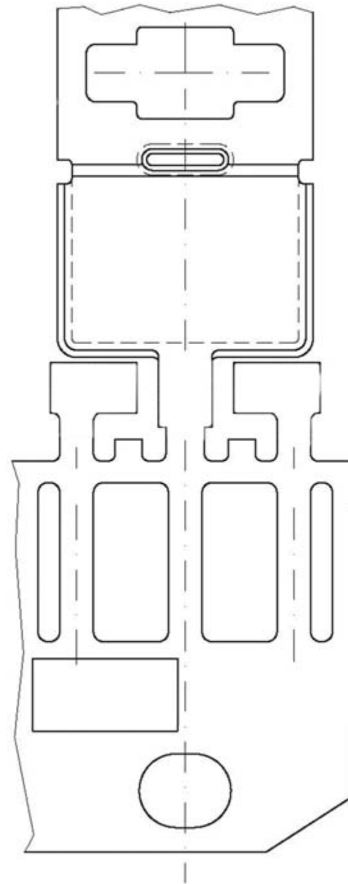
DOCUMENT APPROVAL

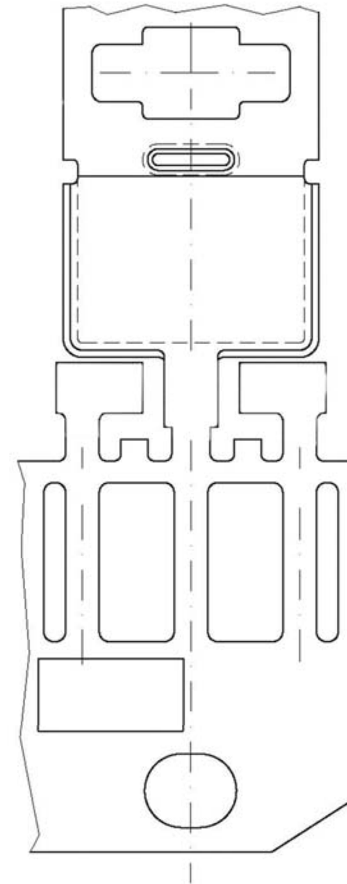
Name	Function
Giudice, Maurizio	Division Marketing Manager
Saya, Francesco	Division Marketing Manager
Aleo, Mario-Antonio	Division Product Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

Single gauge Vs Dual gauge DPAK NO Differences

(front view)

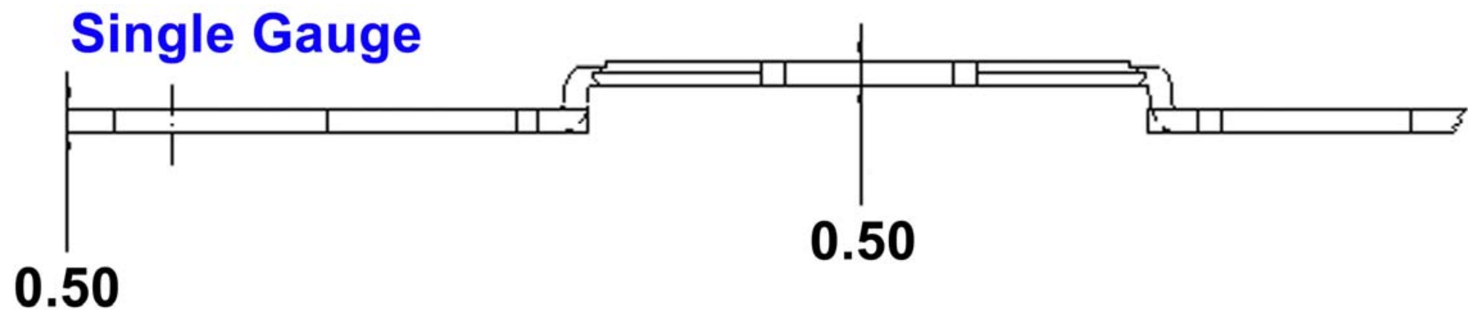
Single Gauge | **Dual Gauge**

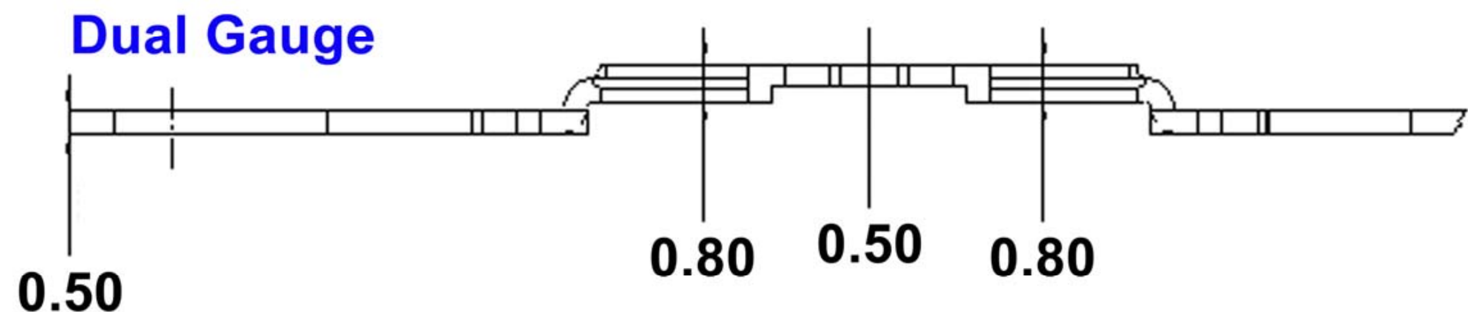




Single gauge Vs Dual gauge DPAK Differences

(side view)





Unit: mm

Reliability Report

On DPAK single gauge made in Shenzhen CHINA

Test Vehicles: STD4NK50ZT4, STD50NH02LT4, MJD122T4

General Information	
Product Line	EZ51
Product Description	Power MOSFET N-channel
Commercial Product	STD4NK50ZT4
Product Group	IMS
Product Division	Power MOSFET
Package Description	DPAK
Silicon Process Technology	SuperMESH™ Power MOSFET

Locations	
Wafer fabrication location	Ang Mokio (Singapore)
Assembly plant location	Shenzhen (China)
Final test plant location	Shenzhen (China)

General Information	
Product Line	3L2C
Product Description	Power MOSFET N-channel
Commercial Product	STD50NH02LT4
Product Group	IMS
Product Division	Power MOSFET
Package Description	DPAK
Silicon Process Technology	STripFET™ III Power MOSFET

Locations	
Wafer fabrication location	M5 (Italy)
Assembly plant location	Shenzhen (China)
Final test plant location	Shenzhen (China)

General Information	
Product Line	BB01
Product Description	Darlington transistor
Commercial Product	MJD122T4
Product Group	IMS
Product Division	Power BIPOLAR
Package Description	DPAK
Silicon Process Technology	PLANAR NPN Power BIPOLAR

Locations	
Wafer fabrication location	Ang Mokio (Singapore)
Assembly plant location	Shenzhen (China)
Final test plant location	Shenzhen (China)

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	March, 2009	**10**	Montalto Gaetano	Original document

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the DPAK single gauge made in Shenzhen (CHINA).

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

STD4NK50ZT4 SuperMESH™ Power MOSFET, STD50NH02LT4 STripFET™ III Power MOSFET, MJD122T4 PLANAR NPN Power BIPOLAR

4.2 Construction note

D.U.T.: STD4NK50ZT4 LINE: EZ51 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	SuperMESH™ Power MOSFET
Die finishing back side	Ti/Ni/Au
Die size	2700 x 2170 µm2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	SINGAPORE Ang Mo Kio
Test program	WPIS

Assembly information	
Assembly site	SHENZHEN (CHINA).
Package description	TO-252 DPAK
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Gate Al/Mg 10 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	SHENZHEN (CHINA).
Tester	IP tester

D.U.T.: STD50NH02LT4 LINE: 3L2C PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*M5 Catania (Italy)*
Technology	STripFET™ III Power MOSFET
Die finishing back side	Ti/Ni/Au
Die size	2500 x 1800 μm^2
Metal	AlSiCu
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	EWS Catania
Test program	WPIS

Assembly information	
Assembly site	SHENZHEN (CHINA).
Package description	TO-252 DPAK
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Gate Al/Mg 10 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	SHENZHEN (CHINA).
Tester	IP tester

D.U.T.: MJD122T4 LINE: BB01 PACKAGE: TO 252 DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (SINGAPORE)*
Technology	PLANAR NPN
Die finishing back side	AuAs/Cr/Ni/Au
Die size	1850 x 1970 µm²
Metal	Al/Si
Passivation type	P-VAPOX

Wafer Testing (EWS) information	
Electrical testing manufacturing location	SINGAPORE Ang Mo Kio
Test program	WPIS

Assembly information	
Assembly site	SHENZHEN (CHINA).
Package description	TO-252 DPAK
Molding compound	Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Base Al/Mg 7 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	SHENZHEN (CHINA).
Tester	IP tester

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STD4NK50ZT4	EZ51	Power MOSFET
2	STD50NH02LT4	3L2C	Power MOSFET
3	MJD122T4	BB01	Power BIPOLAR

5.2 Reliability test plan and results summary

D.U.T.: STD4NK50ZT4 LINE: EZ51 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTSL	N	JESD22 A-103	Ta = 150℃	77	1000H	0/77
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=400V	77	1000H	0/77
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 30V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=100V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77
TF	N	JESD22 A-105-B	∆TC=105℃ - Pd=2W	77	10Kcy.	0/77

D.U.T.: STD50NH02LT4 LINE: 3L2C PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTSL	N	JESD22 A-103	Ta = 175℃	77	1000H	0/77
HTRB	N	JESD22 A-108	T.A.=175℃ Vdd=20V	77	1000H	0/77
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 20V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=20V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77
TF	N	JESD22 A-105-B	ΔTC=105℃ - Pd=2W	77	10Kcy.	0/77

D.U.T.: MJD122T4 LINE: BB01 PACKAGE: TO 252 DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
PRECONDITIONING OF SMD DEVICES	-	JESD22-A113-B	DRYNG 24H @ 125℃ STORE 168H @ TA=85℃ RH=85% Reflow @ 260℃ 3 times	154	Parameter deviation within spec. limits at end of preconditioning	No parameter deviation out of spec. limits at end of preconditioning.
HTSL	N	JESD22 A-103	Ta = 150℃	77	1000H	0/77
HTRB	N	JESD22 A-108	T.A.=150℃ Vdd=80V	77	1000H	0/77
THB	Y	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=100V	77	1000H	0/77
TC	Y	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77	500 cy	0/77
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77	96 H	0/77
TF	N	JESD22 A-105-B	ΔTC=105℃ - Pd=2W	77	10Kcy.	0/77

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF Thermal Fatigue	This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress).	The purpose of this test is to detect assembly defects: improper die-attach, bonding weakness and thermal mismatch among various components of the package.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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