PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/09/4355
Notification Date 02/06/2009

128Kbit Serial I2C Bus EEPROM Redesign and Upgrade to the CMOSF8L Process Technology in ST Rousset 8" fab

Table 1. Change Implementation Schedule

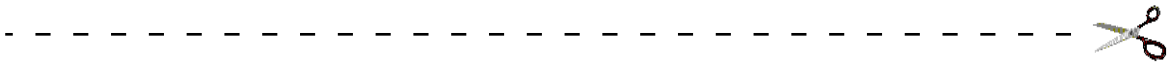
Forecasted implementation date for change	30-Jan-2009
Forecasted availabillity date of samples for customer	30-Jan-2009
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	30-Jan-2009
Estimated date of changed product first shipment	08-May-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	128Kbit I2C products family in SO8N and TSSOP8 pac
Type of change	Waferfab technology change
Reason for change	Production capacity increase and line up to state of art of design.
Description of the change	Redesign and Upgrade to the CMOSF8L Process Technology.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process techno identifer is A, only visible on SO8N package
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/09/4355**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 02/06/2009**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

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PRODUCT / PROCESS CHANGE NOTIFICATION

128Kbit Serial I2C Bus EEPROM
Redesign and Upgrade to the CMOSF8L Process Technology in ST Rousset 8" fab

What is the change?
The **128Kbit** Serial **I2C** Bus EEPROM product family, currently produced using the CMOSF6DP 26% Process Technology in the Chartered subcon. (Singapore) 8 inch wafer diffusion plant has been **redesigned and upgraded** to the **CMOSF8L** Process Technology in the **ST Rousset 8** inch wafer diffusion plant. This PCN impacts the products in SO8N and TSSOP8 packages.

Why?
The strategy of STMicroelectronics Memory Division is to support the growth of our customers on a long-term basis. In line with this commitment, the qualification of the 128Kbit I2C in the ST Rousset 8 inch with the CMOSF8L Process Technology will increase the production capacity throughput and consequently improve the service to our customers.

When?
The production of the upgraded 128K I2C in ST Rousset with the qualified process CMOSF8L is ramping up and shipments in SO8N and TSSOP8 packages can start from March 2009 onward (upon customer approval).
Shipments of newly introduced packages MLP 2x3 (UFDFPN8) and WLCSP (Wafer Level Chip Scale Package) already started 9 months ago.

How will the change be qualified?
The new version of the 128Kbit I2C is qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

The **Qualification Report QREE0720 rev2** is **available** and included inside this document.

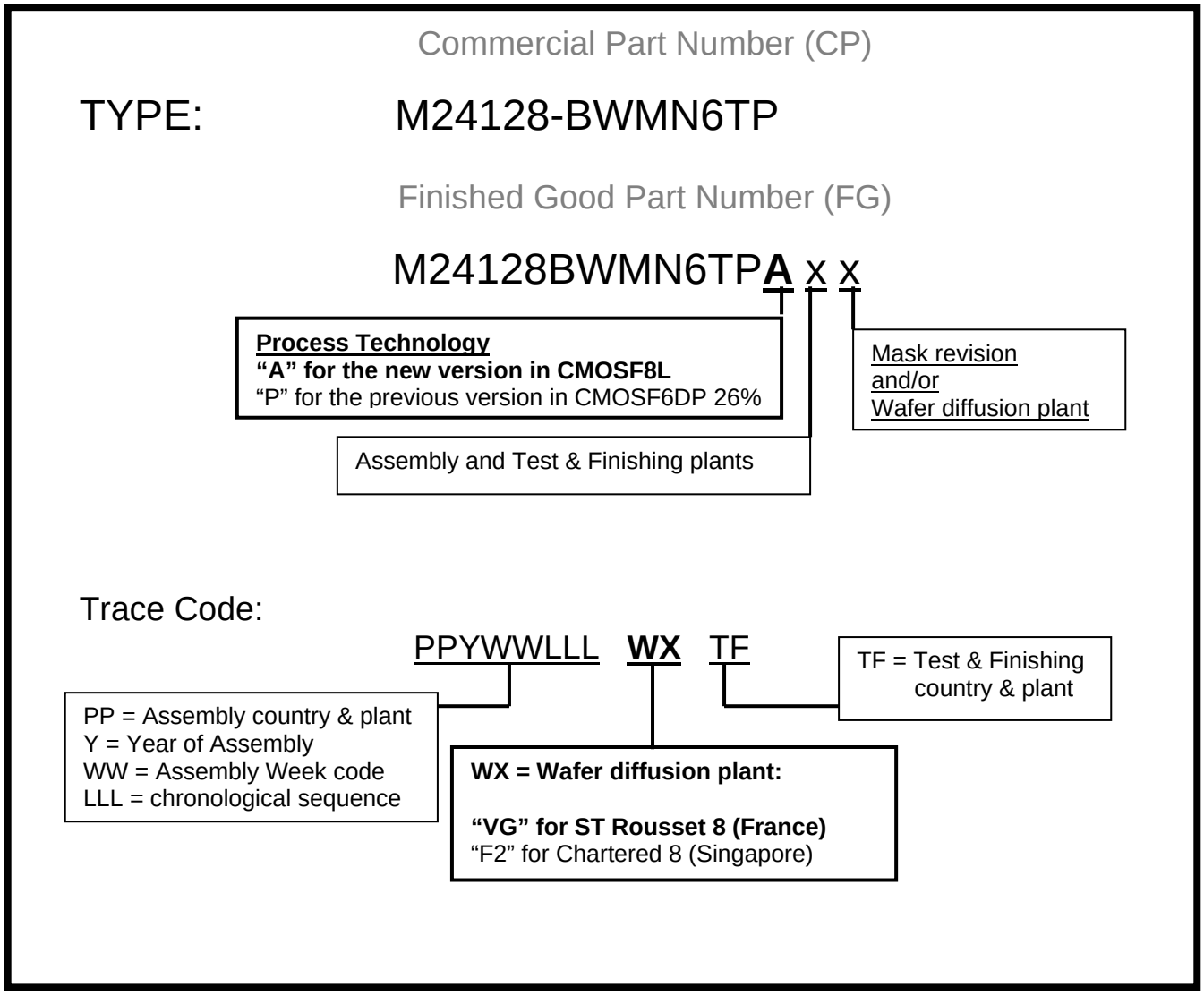
How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the change is visible inside the **Finished Good Part Number**: the **Process Technology** identifier is "**A**" for the **CMOSF8L upgraded version**, this identifier being "P" for the previous version.

The change is also visible inside the **Trace code**: the **Wafer Fab** identifiers WX are "**VG**" for **ST Rousset 8** inch (France), these identifiers being "F2" for Chartered 8 inch subcontractor (Singapore).

➔ *Example for M24128-BWMN6TP (2.5V to 5.5V Vcc range, SO8N ECOPACK2 package)*



How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the **SO8N** package, the change is visible inside the trace code (PYWWT) where the last digit "T" for **Process Technology** identifier is "**A**" for the **upgraded version** in **CMOSF8L**, the identifier being "P" for the previous version in CMOSF6DP26%.

	Upgraded **M24128** **CMOSF8L**	Previous M24128 CMOSF6DP 26%
SO8N Example: M24128-BWMN6TP	24128WP PYWW**A**	24128WP PYWW**P**

The traceability for each device is as follows:

P Y WW T

P = Assembly plant
Y = Last digit of the Year of Assembly
WW = Assembly Week code
T = Process Technology code/ Wafer Fab ID

For **TSSOP8** package size reason, the change is not visible on the device marking. The change is only visible inside the Finished Good Part Number appearing on the BOX LABEL MARKING (See previous page).

Appendix A- Product Change Information

Product family / Commercial products:	128Kbit I2C products family in SO8N and TSSOP8 packages
Customer(s):	All
Type of change:	Wafer fab Process Technology change
Reason for the change:	Production capacity increase and line up to state of art of design.
Description of the change:	Redesign and Upgrade to the CMOSF8L Process Technology.
Forecast date of the change: **(Notification to customer)**	Week 06 / 2009
Forecast date of **Qualification samples availability for customer(s):**	Available
Forecast date for the internal STMicroelectronics change, **Qualification Report availability:**	QREE0720 is available
Marking to identify the changed product:	Process and fab ID see marking above
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See list of concerned products in appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 19 / 2009 (or earlier upon customer approval)

Appendix B: concerned products:

M24128-BRDW6TP
M24128-BRMN6P
M24128-BRMN6TP
M24128-BWDW6TP
M24128-BWMN6P
M24128-BWMN6TP

Appendix C: Qualification Report:

QREE0720
Qualification report

New product / M24128 M24C64
using CMOSF8L technology in Rousset 8" Fab

Table 1. Product information

General information	
Commercial product	M24128-BFMB6TG M24128-BRMB6TG M24128-BWDW6TP M24128-BRDW6TP M24128-BRMN6TP M24128-BRMN6P M24128-BWMN6TP M24128-BWMN6P M24C64-FMB6TG M24C64-RMB6TG
Product description	128 Kbit and 64 Kbit serial I²C bus EEPROM for M24128 and M24C64, respectively.
Product group	MMS
Product division	MMY
Silicon process technology	CMOSF8L
Wafer fabrication location	RS8F - ST Rousset 8", France
Electrical Wafer Sort plant location	ST Rousset, France

Table 2. Package description

Package description	Qualified assembly plant location	Qualified final test plant location
SO8N	Amkor P1, Philippines	Amkor P3, Philippines
TSSOP8	Amkor P1, Philippines	Amkor P3, Philippines
UFDFPN8 (MLP8) 2x3	Amkor P3, Philippines	Amkor P3, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the M24128 / M24C64 products using the CMOSF8L silicon process technology in the ST Rousset 8" diffusion fab.

The voltage and temperature ranges covered by this document are:

- 1.8 to 5.5 V at –40 to 85 °C for M24128-BR and M24C64-R devices
- 2.5 to 5.5 V at –40 to 85 °C for M24128-BW devices
- 1.7 to 5.5 V at –40 to 85 °C for M24128-BF and M24C64-F devices

The CMOSF8L is a new advanced silicon process technology, with Double Poly and Double Metal process that has already been qualified in the Rousset 8" fab. This document serves for the qualification of the named product, using the qualified named silicon process technology in the named diffusion fab.

1.2 Conclusion

The M24128 / M24C64 products using the CMOSF8L silicon process technology in the ST Rousset 8" diffusion fab have passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The M24C64 and M24128 devices are I^2C-compatible electrically erasable programmable memories (EEPROM). They are organized as 8192 × 8 bits and 16384 × 8 bits, respectively.

I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data are read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24128 / M24C64 (1)	CMOSF8L	ST Rousset 8"	CDIP8	Engi assy (2)
M95128 (3)	CMOSF8L	ST Rousset 8"	CDIP8	Engi assy (2)

1. M24C64 is derived from M24128 by CAM option.
2. CDIP8 is a ceramic package used only for die-oriented reliability trials.
3. Qualification results of M95128 are applicable (same silicon process technology, same design core / Metal mask option for bus control).

The package qualifications were mainly obtained by similarity. The product vehicles and silicon process technologies used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95128 (1)	CMOSF8L	ST Rousset 8"	UFDFPN8 (MLP8) 2 x 3 mm	Amkor P3
M95512 (2)	CMOSF8L	ST Rousset 8"	SO8N	Amkor P1
			TSSOP8	Amkor P1

1. Qualification results of M95128 are applicable (same silicon process technology, same design core / Metal mask option for bus control).
2. Qualification results of M95512 are applicable (larger memory array, using the same silicon process technology in the same diffusion fab).

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for UFDFPN8 (MLP8) 2x3 Amkor P3 package-oriented tests
- in *Table 7* for TSSOP8 Amkor P1 package-oriented tests
- in *Table 8* for SO8N Amkor P1 package-oriented tests
- Qualification report QREE0402 summarizes the reliability trials and results that were performed to qualify the Lead-free Nickel Palladium Gold pre-plated frame on MLP8 2 × 3 package in the Amkor P3 assembly line.
- Qualification report QREE0425 summarizes the reliability trials and results that were performed to qualify the CMOSF8L silicon process technology in ST Rousset 8" diffusion fab.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)[1]

Test	Test short description						
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size	
						M95128	M24128 / M24C64
						Lot 1	Lot 2 [2]
EDR	High temperature operating life after endurance						
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTOL at 150 °C, 6 V	80	1	1008 hrs	0/80	-
	Data retention after endurance						
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTSL at 150 °C	80	1	1008 hrs	0/80	-
LTOL	Low temperature operating life						
	JESD22-A108	–40 °C, 6 V	80	1	1008 hrs	0/80	-
HTSL	High temperature storage life						
	JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80	-
WEB	Program/erase endurance cycling + bake						
	Internal spec.	1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	1 Million cycles / 48 hrs	0/80 [3]	0/80 [3]
ESD HBM	Electrostatic discharge (human body model)						
	AEC-Q100-002 JESD22-A114	C = 100 pF, R = 1500 Ω	27	1	N/A	Pass >4000 V	Pass >4000 V
ESD MM	Electrostatic discharge (machine model)						
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	6	1	N/A	Pass >400 V	Pass >400 V
LU	Latch-up (current injection and overvoltage stress)						
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	1	N/A	Class II - Level A	Class II - Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification results of M95128 are applicable (same silicon process technology, same design core / Metal mask option for bus control).
3. First rejects after 5 million cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (UFDFPN8 2×3 / Amkor)[1][2]

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M95128		
						Lot1	Lot2	Lot3
PC	Preconditioning: moisture sensitivity level 1							
	JESD22-A113 J-STD-020C	MSL1, Peak temperature at 260 °C, 3 IReflows	345	3	N/A	0/345	0/345	0/345
THB [3]	Temperature humidity bias							
	AEC-Q100-JESD22-A101	85 °C, 85% RH, Bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80
TC [3]	Temperature cycling							
	AEC-Q100-JESD22-A104	–65 °C/+150 °C	80	3	1000 cycles	0/80	0/80	0/80
TMSK [3]	Thermal shocks							
	JESD22-A106	–55 °C/+125 °C	25	3	200 shocks	0/25	0/25	0/25
AC [3]	Autoclave (pressure pot)							
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80
HTSL [3]	High temperature storage life							
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
ESD CDM	Electrostatic discharge (charge device model)							
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification results of M95128 are applicable (same silicon process technology, same design core / Metal mask option for bus control).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and results summary (TSSOP8 / Amkor P1)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95512			M24128
						Lot1	Lot2	Lot3	Lot4 (2)
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020C	MSL1, peak temperature at 260 °C, 3 IReflow	345	3	N/A	0/345	0/345	0/345	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–65 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500V	-	-	Pass >1500V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification results of M95512 are applicable (larger memory array, using the same silicon process technology in the same diffusion fab).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (SO8N / Amkor P1) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95512			M24128
						Lot1	Lot2	Lot3	Lot4 (2)
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020C	MSL1, Peak temperature at 260 °C, 3 IReflows	345	3	N/A	0/345	0/345	0/345	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, Bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	3	200 shocks	0/25	0/25	0/25	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500V	-	-	Pass >1500V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification results of M95512 are applicable (larger memory array, using the same silicon process technology in the same diffusion fab).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

Document Revision History

Date	Rev.	Description of the Revision
Jan. 26, 2009	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

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