PRODUCT/PROCESS CHANGE NOTIFICATION

PCN HED-TVM/08/4249
Notification Date 12/22/2008

Audio Switches STV6422D & STV6422DT Front end manufacturing location change

Table 1. Change Implementation Schedule

Forecasted implementation date for change	15-Dec-2008
Forecasted availabillity date of samples for customer	15-Dec-2008
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Dec-2008
Estimated date of changed product first shipment	23-Mar-2009

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	Audio Switches STV6422D & STV6422DT
Type of change	Waferfab location change
Reason for change	Carrolton Front end site closure
Description of the change	Following the carrolton Front end site closure decision decided by corporation , the production will be done in AMK .
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Marking
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	**PCN HED-TVM/08/4249**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 12/22/2008**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Loveridge, Graham	Division Marketing Manager
Lauga-larroze, Christophe	Division Product Manager
Mottais, Christian	Division Q.A. Manager

Internal Reliability Qualification Plan

FAB transfer

General Information	
Commercial Product	: TEA6420 TEA6422 TEA6425
Package	: SO20 / SO28
Process	: HF2CMOS
Maturity level (actual)	: MAT10
Maturity level (targeted)	: MAT30

Locations	
Wafer FAB location	: AM6F
Assembly plant location	: MUAR
Reliability LAB location	: GRENOBLE
Reference number	: tvnext850a

REQUESTOR NAME

NAME	FUNCTION	DATE
Christophe LAUGA-LARROZE	Product Marketing Manager	10/12/2008

DISTRIBUTION LIST

NAME	FUNCTION
Didier JAN	HVD & ISS quality & Reliability
Christian MOTTAIS	Product Quality Assurance

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	11/12/2008	9	David ALEO	Original document

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1. APPLICABLE AND REFERENCE DOCUMENTS

1.1 ADCS references

- SOP267 (0076608) Product maturity level
- SOP2610 (0078589) General product qualification procedure
- SOP2611 (0078590) Program management for product qualification
- SOP2614 (0078588) Reliability requirements for product qualification
- SOP2620 (7019108) New Process / New Product Qualification
- 0061692 Reliability tests and criteria for product qualification
- 0018695 Latch-up sensitivity measurement method
- 0060102 Electrostatic discharge sensitivity (ESDS) measurement
- 0098041 SMD Moisture induced stress sensitivity
- 0098044 Preconditioning of SMD
- 7089402 GRENOBLE MMC Reliability laboratory management manual

1.2 Other references

- JESD 22A101 Steady State Temperature Humidity Bias Life Test
- JESD 22A102 Accelerated Moisture Resistance - Unbiased Autoclave
- JESD 22A103 High Temperature Storage Life
- JESD 22A104 Temperature Cycling
- JESD 22A108 Temperature, Bias, and Operating Life
- JESD 22A110 Highly-Accelerated Temperature and Humidity Stress Test (HAST)
- JESD 22A113 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
- JESD 22A118 Accelerated Moisture Resistance - Unbiased HAST
- JESD 47 Stress-Test-Driven Qualification of Integrated Circuits
- JESD 74 Early Life Failure Rate Calculation Procedure for Electronic Components
- JSTD 020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

2. GLOSSARY

PC : Preconditioning
TC : Temperature Cycling
AC : Autoclave
HTSL : High Temperature Storage Life
HTRB : High Temperature Reverse Bias
THB : Temperature Humidity Bias
HTOL : High Temperature Operating Life
HBM : Electrostatic Discharge Human Body Model
MM : Electrostatic Discharge Machine Model
CDM : Electrostatic Discharge Charged Device Model
LU : Latch Up
THS : High Temperature Humidity Storage

NPR : New product request
DAC : Design approval certificate
RER : Reliability Evaluation Report
PQC : Product Qualification Report

3. RELIABILITY EVALUATION OVERVIEW

3.1 OBJECTIVES

This qualification plan intends to define reliability trials required to qualify the new FAB transfer in AM6F for TEA6420, TEA6422 and TEA6425.

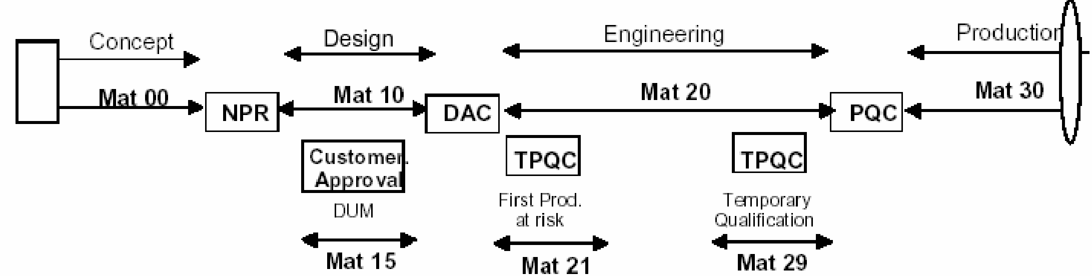
The manufacture conditions are the following:

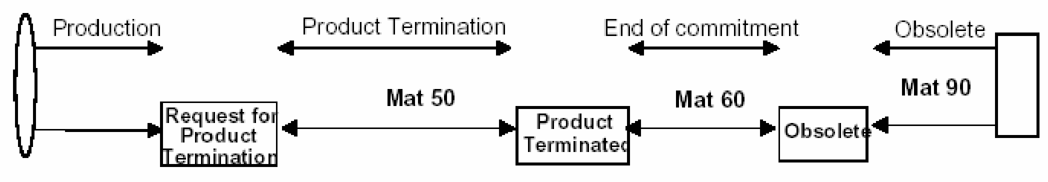
- Process : HF2CMOS from AM6F
- Assembly : TEA 6420 SO28 from MUAR
  TEA 6422 SO28 from MUAR
  TEA 6425 SO20 from MUAR

3.2 MATURITY FLOW

Part I: Introduction and growth to Maturity

Part II: Maturity to Saturation, decline and obsolescence





4. DEVICE CHARACTERISTICS

4.1 TRACEABILITY

4.1.1 Wafer fab information

4.1.1.1 TEA 6420 / TEA6422 / TEA6425

Wafer FAB information	description
Wafer FAB	AM6F
Process	HF2CMOS
Wafer thickness	375µm
Die finish front side	P-VAPOX(SiO2) / NITRIDE
Die finish back side	Raw silicon
Min bond pad pitch	110µm
Staggered pads	NO
Pad opening	100 x 100 µm

Wire bond pads metal	composition	Thickness
Metal1	AlSiCu	0.6 µm
Metal2	AlSiCu	1.05 µm

4.1.2 Assembly information

4.1.2.1 TEA6420 / TEA6422

Assembly information	Description
Assembly site	MUAR
Package type	SO 28
Package size	JEDEC MS-013
Glue	HITACHI EN4900 ST12 10ml/35g Sy
Resin	SUMITOMO EME7026 D14.0mm W6.5g
Wire	Au D1.2 BL13-20g EL2-7% sp2x2 2000m
Frame	5FT34308 FRAME SO 28L 150x150 MtxW FloOpA NiPdAu

4.1.2.2 TEA 6425

Assembly information	Description
Assembly site	MUAR
Package type	SO 20
Package size	JEDEC MS-013
Glue	HITACHI EN4900 ST12 10ml/35g Sy
Resin	SUMITOMO EME7026 D14.0mm W6.5g
Wire	Au D1.3 BL>12g EL4-8% spF 1000m
Frame	5FT44632 FRAME SO 20L 195x230 Flo NiPdAu

4.1.3 Reliability equipment information

Designation	Description	Type	Supplier	Verification	User manual
Human Body Model Machine Model	ESD	MK2	THERMO	ADCS n°0049955	Supplier user manual
Charge Device Model	ESD	CDM	THERMO	ADCS n°7470943	
Latch Up	LU	MK2	THERMO	ADCS n°0049955	

5. RELIABILITY TESTS PLAN

Die oriented tests

Description	abv	Reference	Condition	Test Intervals	Sample size	Comments
Human Body Model	HBM	ADCS 0060102 (JESD22-A114)	3/pin combo model +/- 2000V	Before and after stress	3 parts per combo	
Machine Model	MM	ADCS 0060102 (JESD22-A115)	3/pin combo model +/- 200V	Before and after stress	3 parts per combo	
Charge Device Model	CDM	ADCS 0060102 (ANSI/ESD STM5.3.1)	3 parts per level Limit determination	Before and after stress	3 parts per combo	
Latch Up	LU	ADCS 0018695	Current injection Overvoltage	Before and after stress	10	Stress at 25°C and 125°C

6. TESTS DESCRIPTION

6.1 DIE ORIENTED TESTS

Die oriented tests

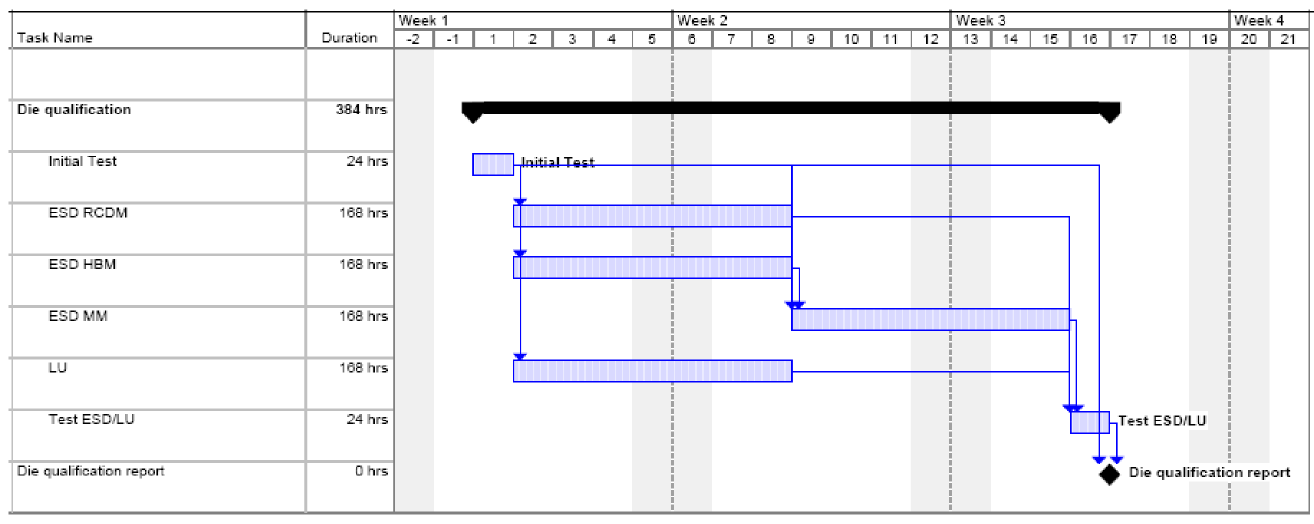
Description	abv	reference	Test Intervals
Human Body Model	HBM	ADCS 0060102 (JESD22-A114)	Test methods according to spec 0060102.This testing is performed to evaluate the device immunity to Electro-Static Discharges (ESD). Three generalized models have been suggested for ESD events that can cause device damage or failure. The HBM model approximates the discharge from the fingertip of a typical human being. A 100 pF capacitor is charged to Vstress and then discharged through a 1500 ohm series resistor into the pin under test (PUT).
Charge Device Model	CDM	ADCS 0060102 (ANSI/ESD STM5.3.1)	Test methods according to spec 0060102.This testing are performed to evaluate the device immunity to Electro-Static Discharges (ESD). Three generalized models have been suggested for ESD events that can cause device damage or failure. The CDM model is intended to simulate charging / discharging events that occur in production equipment and processes. The Field induced CDM equivalent circuit used to describe this phenomenon is illustrated in **Figure 1**.

Die oriented tests

Description	abv	reference	Test Intervals
Machine Model	MM	ADCS 0060102 (EIA/JEDEC A115A)	A test method according to spec 0060102.This testing is performed to evaluate the device immunity to Electro-Static Discharges (ESD). Three generalized models have been suggested for ESD events that can cause device damage or failure. The simulation test approximates the electrostatic discharge from a machine. The Machine Model is virtually the same as the HBM except the discharge is through a very low resistance. This results in a faster, higher-current pulse. The equivalent circuit for the machine model is similar to the HBM, except that the body resistance is lower (0 Ohm) and a series inductance (200pF) should be included (since it will have a dramatic effect on the pulse). Experience with the proposed standard models has shown that the MM produces failure models similar to those seen in HBM testing
Latch Up	LU	ADCS 0018695	This trial will be done in order to determine the product latch-up sensitivity according to specification n°0018695. • Over-voltage: this test simulates an user induced situation where a transient over-voltage is applied on power supplies. • Current injection: this test simulates an user or application induced situation where either applied voltages on any pin is greater than Vcc or where severe overshoot occurs on inputs.

7. RELIABILITY QUALIFICATION SCHEDULE

7.1.1 Reliability Evaluation



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