PRODUCT/PROCESS CHANGE NOTIFICATION

PCN HED-AUD/08/4167
Notification Date 11/14/2008

TDA7438D; TDA7439DS; TDA7440D; TDA7449D DIFFUSION TRANSFER FROM CARROLTON 6" TO ANG MO KIO 6"

Table 1. Change Implementation Schedule

Forecasted implementation date for change	07-Nov-2008
Forecasted availabillity date of samples for customer	07-Nov-2008
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	07-Nov-2008
Estimated date of changed product first shipment	19-Dec-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	A563 line in SO package
Type of change	Waferfab location change
Reason for change	Carrolton Fab Closure
Description of the change	Following the APCN CRP/07/3289 dated 12/28/2007 ST is transferring the devices TDA7438D; TDA7439DS; TDA7440D; TDA7449D , all belonging to the A563 silicon line (HF2CMOS S baseline 475A gate front-end technology) from the diffusion plant in Carrolton (USA) to the diffusion plant in Ang Mo Kio (Singapore). TIME SCHEDULE SUBJECT TO CUSTOMER APPROVAL
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Plant marking identification "V6" for Ang Mo Kio plant
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	**PCN HED-AUD/08/4167**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 11/14/2008**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Angelici, Marco	Division Marketing Manager
Onetti, Andrea Mario	Division Product Manager
Piccoli, Massimo	Division Q.A. Manager

TDA7438D; TDA7439DS; TDA7440D; TDA7449D DIFFUSION TRANSFER FROM CARROLTON 6” TO ANG MO KIO 6”

WHAT

Following the APCN CRP/07/3289 dated 12/28/2007 ST is transferring the devices TDA7438D; TDA7439DS; TDA7440D; TDA7449D , all belonging to the A563 silicon line (HF2CMOS S baseline 475A gate front-end technology) from the diffusion plant in Carrolton (USA) to the diffusion plant in Ang Mo Kio (Singapore).
All the mentioned devices are assembled in SO package family.

WHY

In order to optimize ST asset utilization and enhance performance for shareholders and customers.

HOW

The mentioned front-end technology has been re-qualified in the receiving plant trough the evaluation of TDA7440D as test vehicle (A563 silicon line assembled in SO28 package).
Following the report with qualification results.

Reliability Report

Diffusion plant transfer

General Information	
Product Line	*A563*
Product Description	*THREE BAND AUDIO PROCESSOR*
Commercial Product	*TDA7440D*
Product Group	*HED*
Product division	*AUDIO*
Package	*SO 28*
Silicon process technology	*HF2CMOS SHRINK*

Locations	
Wafer fab location	*AMK 6*
Assembly plant location	ST MUAR - MALAYSIA
Reliability assessment	*Passed*

Issued by Fabio Pietro Fiabane

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluation performed on *A563* in order to release the device to production volume.

A563 is processed in *HF2CMOS SHRINK,* diffused in *AMK 6,* and assembled in *SO28* in *ST MUAR - MALAYSIA*.
For the reliability evaluation the following tests were carried out:
AC, HTOL, HTSL, TC, ESD, LATCH UP.

1.2 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die oriented test showed a good stability of the main electrical monitored parameters.
Package oriented tests have not put in evidence any criticality.
ESD & Latch-Up are in accordance with ST spec.

On the ground of the overall positive results we can conclude that *A563* device can be qualified from a reliability point of view.

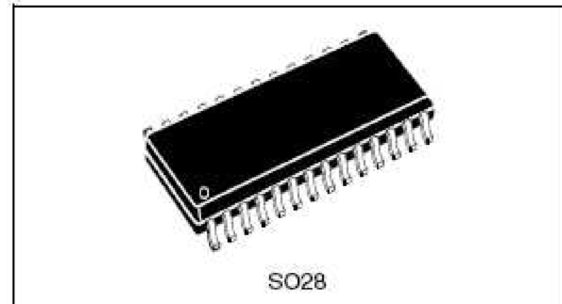
2 DEVICE CHARACTERISTICS

2.1 Device description

Three-band digitally-controlled audio processor

Features

- Input multiplexer
  - four stereo inputs
  - selectable input gain for optimal adaptation to different sources
- Single stereo output
- Treble, mid-range and bass control in 2-dB steps
- Volume control in 1-dB steps
- Two speaker attenuators:
  - two independent speaker controls in 1-dB steps for balance facility
  - independent mute function
- All functions are programmable via serial bus.


SO28

Description

The TDA7439DS is a volume, tone (bass, mid-range and treble) and balance (left/right) processor for quality audio applications in car-radio and Hi-Fi systems. Selectable input gain is provided. All the functions are controlled by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

The TDA7439DS employs BIPOLAR/CMOS technology to provide low distortion, low noise and DC stepping.

2.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*AMK 6*
Silicon process technology	*HF2CMOS SHRINK*
Die size	*2840 x 2250 micron*
Passivation	*P-VAPOX(SiO2) / NITRIDE (SiN)*
Die finishing back side	*Raw Silicon*

Assembly Information	
Assembly plant location	*ST MUAR - MALAYSIA*
Package description	*SO 28 .30 TO JEDEC MS-013AE*
Frame	*FRAME SO 28L 150x200 NiPdAu*
Die attach process	*Glue*
Die pad size	*3.81 x 5.08 mm*
Molding compound	*Sumitomo 7026*
Wires bonding materials/diameters	*Au (1.2 mils)*
Die attach material	*Glue Hitachi EN4900*

3 RELIABILITY TESTS RESULTS

3.1 Test plan and results summary

3.1.1 Relaibility tests

N	TEST NAME	PREC	CONDITION/METHOD	STEPS	FAILS/SS			NOTES
					LOT 1	LOT 2	LOT 3	
1	**Preconditioning (Jedec Level 3)**		REFLOW PROFILE = J-STD-020C Moisture Sensitivity 3 (1 Week at <=30℃/60%RH) (Peak body Temperature=260℃)	FINAL	0/300	0/300	0/300	
2	**HTOL**	Y	Vcc=10.2V, Tj = 150℃	168 H	0/77	0/77	0/77	
				500 H	0/77	0/77	0/77	
				1000 H	0/77	0/77	0/77	
3	**HTSL**	N	Ta = 150℃	500 H	0/77	0/77	0/77	
				1000 H	0/77	0/77	0/77	
4	**TC**	Y	Ambient Temp Range = -50℃/150℃	500 Cy	0/77	0/77	0/77	
				1000 Cy	0/77	0/77	0/77	
5	**AC**	Y	Pa / Ta = 2 Atm / 121℃	168 H	0/77	0/77	0/77	
6	**ESD HBM**	N	JEDEC / JESD22-A114E VOLTAGE +/-2000V	-	0/3			
7	**ESD MM**	N	JEDEC / JESD-A115-A VOLTAGE +/-200V	-	0/3			
8	**ESD CDM**	N	ANSI / ESD STM 5.3.1 ESDA VOLTAGE +/-750v	-	0/3			
9	**Latch Up and Overvoltage**	N	EIA/JESD78 LEVEL A (+/-200mA) 1.5 x Vmax	-	0/12			

3.1.2 Manufacturing control tests

N	TEST NAME	PREC	CONDITION/METHOD	STEPS	FAILS/SS			NOTES
					LOT 1	LOT 2	LOT 3	
1	**Solderability**	N	ST internal spec 0018688 rev. W JEDEC / JESD22b102d solderability std	FINAL	0/15	0/15	0/15	

3.2 Die and Package tests description

TEST NAME	DESCRIPTION	PURPOSE
AC: Autoclave at 2atm	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity
HTOL: High Temperature Operating Life	The device is stressed in dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature, load current, internal power dissipation.	To simulate the worst-case application stress conditions. The typical failure modes are related to electromigration, wire-bonds degradation, oxide faults.
HTSL: High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
PC (JL3): Preconditioning (solder simulation)	The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.	As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TC: Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die
ESD (HBM): Electrostatic Discharge (Human Body Model)	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models.	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
ESD (MM): Electrostatic Discharge (Machine Model**)**	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
ESD (CDM): Electrostatic Discharge (Charged Device Model)	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU (CI): Latch-up (Overvoltage and Current Injection)	The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effects inducing latch-up.

4 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for integrated circuits
SOP 2.6.10	General product qualification procedure
SOP 2.6.11	Program management fro product qualification
SOP 2.6.12	Design criteria for product qualification
SOP 2.6.14	Reliability requirements for product qualification
SOP 2.6.19	Process maturity level
SOP 2.6.2	Process qualification and transfer management
SOP 2.6.20	New process / New product qualification
SOP 2.6.7	Product maturity level
SOP 2.6.9	Package and process maturity management in Back End
SOP 2.7.5	Automotive products definition and status

5 TEST GLOSSARY

TEST NAME	DESCRIPTION	NOTE
AC	Autoclave at 2atm	
HTOL	High Temperature Operating Life	
HTSL	High Temperature Storage Life	
PC (JL3)	Preconditioning (solder simulation)	1
TC	Temperature Cycling	
ESD	Electrostatic Discharge	
LU	Latch Up	

NOTE:
1) To be done before HTOL, AC, TC

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