



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-SLI/08/4023
Notification Date 09/16/2008

**HF5CMOS PROCESS DIFFUSION TRANSFER FROM CARROLLTON TO
SUBCON UMC TAIWAN PLANT 8E**

Table 1. Change Implementation Schedule


Forecasted implementation date for change	08-Dec-2008
Forecasted availability date of samples for customer	09-Sep-2008
Forecasted date for STMicroelectronics change Qualification Plan results availability	09-Sep-2008
Estimated date of changed product first shipment	16-Dec-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Waferfab location change
Reason for change	FAB CLOSURE AS PER CORPORATE APCN APM-SLI/07/3293
Description of the change	This document is related to the HF5CMOS technology transfer from Carrollton to Subcontractor UMC8E Taiwan and provide details applicable to the products listed in attachment.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	"LE" as identification for UMC plant 8E
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

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Customer Acknowledgement of Receipt		PCN APM-SLI/08/4023
Please sign and return to STMicroelectronics Sales Office		Notification Date 09/16/2008
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark		

DOCUMENT APPROVAL

Name	Function
Gilot, Yves	Division Marketing Manager
Kaire, Jean-Claude	Division Product Manager
Paccard, Francoise	Division Q.A. Manager

HF5CMOS PROCESS DIFFUSION TRANSFER FROM CARROLLTON TO SUBCON UMC TAIWAN PLANT 8E

WHAT:

Progressing along the Restructuring Plan already communicated by Corporate Information Letter (C.I.L.) CRP/07/2927 dated September 25, 2007 and APCN APM-SLI/07/3293 dated December 28, 2007, please be informed that the products currently manufactured in Carrollton 6" Plant (Texas) by using HF5CMOS, will be moved to our subcontractor UMC plant 8E located in Taiwan.

The affected products are listed in the table here attached.

All the products manufactured by ST using HF5CMOS, even if not expressly included in the above mentioned table, are affected by this change.

WHY:

In order to optimize ST asset utilization and enhance performance for shareholders and customers.

HOW:

By transferring and re-qualifying the mentioned front- end technology in the receiving plant; this technology has been qualified through a full set of evaluations on the selected test vehicle (TV for technology qualification): T84, EWS, electrical characterization, die and package oriented stress tests; others products diffused in the same Technology will be qualified mainly by similarity (generic data) if assembled in the same package family. In case of different package families, stress test package oriented will be carried on a "package test vehicle" (FE/BE compatibility) as listed in the annexed table.

Techno family	Product	Package	Product Group	Qualification Plan
HF5CMOS	V912	SO	APM	TV for technology

This transfer will not modify the electrical, dimensional and thermal parameters for the product affected, maintaining unchanged current information published on the relevant datasheets.

There is as well neither change in the packing modes nor in the standard delivery quantities either.

The table here in appendix 1, is providing you the detailed qualification plan that has been used in the new location to qualify the affected test vehicle.

ST will focus on customer satisfaction and ensure a seamless transition in the supply of products from different sites.

WHEN:

The transfer of all product lines and the ramp up in the new location will be finalized within Q1 2009.

Qualification program and results availability:

The qualification program mainly consists of comparative electrical characterizations and reliability tests. The relevant reliability report is provided in appendix 1 of this document.

Samples availability:

Samples of the test vehicle used to qualify the HF5CMOS Technology in our subcontractor UMC 8E facility are already available, while for all the concerned products, samples will be available upon request to the relevant product Business Unit.

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability as indicated in the schedule below:

Product Family Code	Product Family Description	PCN date	1st Shipments
71	Standard Linear	Week 37-2008	From Week 50-2008

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).


In any case, first shipments may start earlier with customer's written agreement.

Product's traceability:

Unless otherwise stated by customer specific requirement, new parts produced in AMK6 will have a differentiated as indicated below:

Diffusion plant	ID	Country of origin
Carrollton (current)	VH	Texas
UMC 8E	LE	Taiwan

Shipments from new Wafer FAB location will be tracked on the ST Standard Label as showed below:

STMicroelectronics	Manufactured under patents or patents pending		
	Assembled in: 1234567890123456		
	Pb-free	2nd Level Interconnect	
	MSL: 12	Bag seal date: dd mm yyyy	
	PBT: 260 C	Category: xx ECOPACK/RoHS	
	TYPE:	1234567890123456 1234567890123456	
	Total Qty:	12345	
	Trace codes	PPYWWLL1	WX TF
		PPYWWLL2	WX TF
	Marking	12345678901234567890	
Bulk ID	1234567890123		
			
Please provide the bulk ID for any inquiry			

Generic ST Standard label

Wafer FAB area code will change from: **VH** to: **LE**

Please note that ST Team is doing all the best for providing you full visibility about the announced restructuring Plan and to minimize any negative impact it may occurs.

While our Marketing and Sales teams are available for additional information when required, we are looking forward to your renewed confidence in STMicroelectronics as the strategic partner of your choice.

Sincerely Yours.

Appendix 1: Reliability tests for qualification program.

Reliability Report

*On HF5CMOS
Test Vehicle: V91201*

General Information		Locations	
Product Line	V91201	Wafer fabrication location	UMC 8E Taiwan
Product Description	Rail-to-rail high output current dual operational amplifier	Assembly plant location (SO8)	Bouskoura Morocco
Commercial Product	TSV912ID / TSV912IS	Final test plant location (SO8)	Bouskoura Morocco
Product Group	LINEAR & INTERFACE	Assembly plant location (Mini SO8)	Carsem Malaysia
Product Division	IMS - APM GROUP	Final test plant location (Mini SO8)	Muar Malaysia
Package Description	SO8 / MiniSO8		
Silicon Process Technology	HF5CMOS		

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
0.1	September-5	4	O. Girard F. Paccard	Original document

Reliability is the attitude of element to satisfy required function in fixed conditions during established time.

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on V912 device used as test vehicle in order to qualify HF5CMOS diffused in UMC 8E.

This product is assembled in SO8 at Bouskoura (Morocco), and in MiniSO8 at Carsem (Malaysia).

Qualification is based upon one lot only because HF5CMOS is already running in UMC8E on a telecom specific device.

1.2 Conclusion

The final reliability results are positive for all stressed lots.

2 DEVICE CHARACTERISTICS

2.1 Device description

The TSV911/2/4 family of single, dual and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

This family features an excellent speed/power consumption ratio, offering an 8 MHz gain bandwidth product while consuming only 1.1mA max at 5V supply voltage. These op-amps are unity gain stable for capacitive loads up to 200 pF.

They also feature an ultra-low input bias current.

These characteristics make the TSV911/2/4 family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

2.2 Traceability

2.2.1 Wafer fabrication information

- Wafer fabrication manufacturing location: UMC 8E in Taiwan
- Technology: HF5CMOS
- Die size: 1.07 mm x 1.1 mm
- Passivation type: PSG / SiN

2.2.2 Assembly information

Assembly site	Bouskoura Morocco	Carsem Malaysia
Package description	SO8	MiniSO8
Frame	Cu 2.4 x 3.2 mm 8leads	Cu 2.4 x 1.7 mm 8leads
Wire	Au 1 mils	Au 1 mils

3 RELIABILITY TESTS RESULTS

3.1 Reliability test plan and results summary

Die oriented test

Test	Test short description				
	Method	Conditions	Sample size	Duration	Fail/ tested
HTB	High Temperature Bias				
		Tj=150C Vs=absolute max rating	78 x 1 Lot (in SO8)	1000 H	0/78

Package oriented test

Test	Test short description				
	Method	Conditions	Sample size	Duration	Fail/ tested
Env. Seq.	Environment sequence (Thermal Cycle followed by Pressure Pot)				
		TC: Ta =-65°C to 150°C thermal cycle PPT: Ta=121°C – Pa=2 atm	78 x 1 Lot (in SO8)	TC 100 cy PPT 96 H	0/78
G. L.	Gate Leakage stress				
		3 units/lot @ Ta = 155°C +400 Volt 3 units/lot @ Ta = 155°C -400 Volt	6 x 1 Lot (in SO8)	As per AECQ100	0/6

ESD tests

ESD Model	Date	Batch #	Stress voltage (V)	Fail / tested
HBM	May 7th, 2008	LE749008	5000	0 / 3
MM	May 7th, 2008	LE749008	400	0 / 3
CDM	May 7th, 2008	LE749008	1500	0 / 3

All test above are compliant with below standards:

- MIL883C
- JEDEC JESD22
- ANSI ESD STM 5.1

ESD results on samples from receiving plant are aligned with results obtained on sending plant samples.

3.2 Die oriented tests

These tests are performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and reverse biased.

The purpose of this test is to detect surface defects such as poor passivation, presence of contaminants, metal corrosion, etc

3.3 Package oriented tests

These tests are performed in order to check device life in various environmental conditions in an accelerated way.

Detectable failure mechanisms are metal corrosion and molding defect, cracking of die, breaking of wire bonding, and mechanical damage to the device case.

4 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for integrated circuits
SOP 2610	General product qualification procedure
Internal ST specification	Reliability Tests and criteria for qualifications (Corporate Q&R rules)
...	

5 GLOSSARY

ESD	Electro Static Discharge
ELFR	Early Life Failure Rate
GL	Gate Leakage
HTB	High Temperature Bias
HTS	High Temperature Storage
T.H.B.	Temperature Humidity Bias
T.C.	Thermal Cycle
P.P.	Pressure Pot
P.C.	Preconditioning
S.M.D.	Surface Mount Device moisture induced stress

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