PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-PMT/08/4005
Notification Date 09/05/2008

TO-220 Assy & Test Location Transfer Ain Sebaa to Bouskoura

Table 1. Change Implementation Schedule

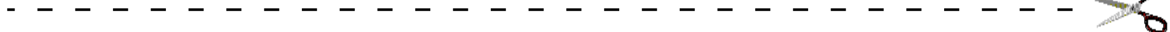
Forecasted implementation date for change	27-Nov-2008
Forecasted availabillity date of samples for customer	29-Aug-2008
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	29-Aug-2008
Estimated date of changed product first shipment	05-Dec-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly location change
Reason for change	Ain-Sebaa (Morocco) plant closure
Description of the change	Progressing along the Restructuring Plan already communicated by Corporate Information Letter CRP/07/2927 dated September 25, 2007 and APCN APM/07/3272, please be informed that the manufacturing lines for products housed in TO-220 package, currently located in AIN-SEBAA (Morocco), are being moved to the Bouskoura site.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	See "CZ" on trace code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM-PMT/08/4005**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 09/05/2008**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Giudice, Maurizio	Division Marketing Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

ST- RELIABILITY EVALUATION PLAN AND RESULTS BASED ON AEC Q101 GUIDE LINES

Device Type: STP80NF55 - 08
Spec # STP80NF55 - 08
Package: TO220
Silicon Line : AD5H

General specification AEC Q101
Supplier: STMicroelectronics
Manufacturing sites: ST, AMK / BOUSKOURA
Family Type: Power MOSFET

pms 25072008_3

Test #	Test Name	Test description	AEC Q101 S.S.	Test Condition	Used S.S.	Results (r/ss)	Family Data (r/ss)
1 & 4	Parametric Verification	Pre and post stress Electrical Verification	All devices submitted to stress steps	Device Type Data Sheet	462	0/462	na
5	HTRB	High Temperature Reverse Bias	77 x 1 Lot	TA=175°C – BIAS=32V TIME=1000 HOURS	77	0/77	0/2060
6	HTGB	High Temperature Reverse Bias	77 x 1 Lot	TA=150°C – BIAS=20V TIME=1000 HOURS	77	0/77	0/260
2	PC	SMD Preconditioning	Not applicable	Not applicable	na	na	na
9	H3TRB	Temperature Humidity Reverse Bias	77 x 1 Lot	TA=85 – RH=85% - BIAS=24V TIME=1000 HOURS	77	0/77	0/2060
10	IOL	Intermittent Operating Life	77 x 1 Lot	T on/off=3.5min ; 8.6Kcycles	77	0/77	0/2060
8	AC	Autoclave	77 x 1 Lot	TA=121°C – PA=2ATM TIME=96h	77	0/77	0/2500
7	TC	Temperature Cycling	77 x 1 Lot	Ta = (-55°C / +150)°C 1Hour x Cycle / 1000Cycle	77	0/77	0/2060
3	EV	External Visual	All devices submitted to stress steps	External Visual	462	0/462	na
13	PD	Physical Dimensions	30 x 1 Lot	Physical Dimensions	30	0/30	0 / >2400
14	LI (TS)	Lead Integrity	45 leads from a minimum of 5 devices x 1 lot	Lead Integrity	15	0/15	0 / >1200
23	BPS	Bond Pull Strength	30 bonds from a min. of 5 devices x 1 lot	Bond Pull Strength	15	0/15	0 / >1200
24	BS	Bond Shear	30 bonds from a min. of 5 devices x1lot	Bond Shear	15	0/15	0 / >1200
21	SD	Solderability	15 x 1 lot	Solderability	15	0/15	0 / >1200
12	DPA	Destructive Physical Analysis	2 x 2 x1 lot	2pcs from H3TRB 2pcs from TC	4	0/4	0 / >320
25	DS	Die Shear	Not applicable	Not applicable			
22	TR	Thermal Resistance	100% Screening	By Delta Vsd	100%	100%	
15	RS	Resistance to Solvent	Not applicable	Laser Marking			

ST- RELIABILITY EVALUATION PLAN AND RESULTS BASED ON AEC Q101 GUIDE LINES

Device Type: STP85NF55L
Spec # STP85NF55L
Package: TO220
Silicon Line : E35H

General specification AEC Q101
Supplier: STMicroelectronics
Manufacturing sites: ST, AMK / BOUSKOURA
Family Type: Power MOSFET

pms 25072008_2

Test #	Test Name	Test description	AEC Q101 S.S.	Test Condition	Used S.S.	Results (r/ss)	Family Data (r/ss)
1 & 4	Parametric Verification	Pre and post stress Electrical Verification	All devices submitted to stress steps	Device Type Data Sheet	462	0/462	na
5	HTRB	High Temperature Reverse Bias	77 x 1 Lot	TA=175°C – BIAS=32V TIME=1000 HOURS	77	0/77	0/2060
6	HTGB	High Temperature Reverse Bias	77 x 1 Lot	TA=150°C – BIAS=20V TIME=1000 HOURS	77	0/77	0/260
2	PC	SMD Preconditioning	Not applicable	Not applicable	na	na	na
9	H3TRB	Temperature Humidity Reverse Bias	77 x 1 Lot	TA=85 – RH=85% - BIAS=24V TIME=1000 HOURS	77	0/77	0/2060
10	IOL	Intermittent Operating Life	77 x 1 Lot	T on/off=3.5min ; 8.6Kcycles	77	0/77	0/2060
8	AC	Autoclave	77 x 1 Lot	TA=121°C – PA=2ATM TIME=96h	77	0/77	0/2500
7	TC	Temperature Cycling	77 x 1 Lot	Ta = (-55°C / +150)°C 1Hour x Cycle / 1000Cycle	77	0/77	0/2060
3	EV	External Visual	All devices submitted to stress steps	External Visual	462	0/462	na
13	PD	Physical Dimensions	30 x 1 Lot	Physical Dimensions	30	0/30	0 / >2400
14	LI (TS)	Lead Integrity	45 leads from a minimum of 5 devices x 1 lot	Lead Integrity	15	0/15	0 / >1200
23	BPS	Bond Pull Strength	30 bonds from a min. of 5 devices x 1 lot	Bond Pull Strength	15	0/15	0 / >1200
24	BS	Bond Shear	30 bonds from a min. of 5 devices x1lot	Bond Shear	15	0/15	0 / >1200
21	SD	Solderability	15 x 1 lot	Solderability	15	0/15	0 / >1200
12	DPA	Destructive Physical Analysis	2 x 2 x1 lot	2pcs from H3TRB 2pcs from TC	4	0/4	0 / >320
25	DS	Die Shear	Not applicable	Not applicable			
22	TR	Thermal Resistance	100% Screening	By Delta Vsd	100%	100%	
15	RS	Resistance to Solvent	Not applicable	Laser Marking			

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