



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MIC/08/3771
Notification Date 06/17/2008

Silicon change for 32K devices of STM32 family

MIC - MICROCONTROLLERS

Table 1. Change Implementation Schedule

Forecasted implementation date for change	30-Jun-2008
Forecasted availability date of samples for customer	10-Jun-2008
Forecasted date for STMicroelectronics change Qualification Plan results availability	30-Jun-2008
Estimated date of changed product first shipment	10-Sep-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See page 7
Type of change	Product design change
Reason for change	Power consumption improvement
Description of the change	We have improved the power consumption of all our STM32 products with a 32 KB Flash memory (both Access and Performance Lines). This makes the STM32 family even better suited to power-sensitive applications. Please refer to the tables on pages 5 to 7 for further details concerning this improvement in the different operating modes (Run and Low-power). As a result of this change, new orderable part numbers have been created that will replace the currently ordered part numbers (see page 7).
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Part number ends with "A"
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Colonna, Daniel	Division Marketing Manager
Nicholas, Jimmy Edward	Division Product Manager
Narche, Pascal	Division Q.A. Manager

Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f _{HCLK}	Max[1]				Unit
				Before		After		
				T _A = 85 °C	T _A = 105 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Run mode	External clock[2], all peripherals enabled	72 MHz	50	50.3	45	46	mA
			48 MHz	36.1	36.2	32	33	
			36 MHz	28.6	28.7	26	27	
			24 MHz	19.9	20.1	18	19	
			16 MHz	14.7	14.9	13	14	
			8 MHz	8.6	8.9	7	8	
		External clock[2], all peripherals disabled	72 MHz	32.8	32.9	30	31	
			48 MHz	24.4	24.5	23	24	
			36 MHz	19.8	19.9	19	19.5	
			24 MHz	13.9	14.2	13	14	
			16 MHz	10.7	11	10	11	
			8 MHz	6.8	7.1	6	7	

[1]Data based on characterization results, not tested in production.

[2]External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.

Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f _{HCLK}	Max				Unit
				Before		After		
				T _A = 85 °C[3]	T _A = 105 °C[2]	T _A = 85 °C[3]	T _A = 105 °C[2]	
I _{DD}	Supply current in Sleep mode	External clock[1], all peripherals enabled	72 MHz	30	32	26	27	mA
			48 MHz	20	20.5	17	18	
			36 MHz	15.5	16	14	15	
			24 MHz	11.5	12	10	11	
			16 MHz	8.5	9	7	8	
			8 MHz	5.5	6	4	5	
		External clock[1], all peripherals disabled	72 MHz	7.5	8	7.5	8	
			48 MHz	6	6.5	6	6.5	
			36 MHz	5	5.5	5	5.5	
			24 MHz	4.5	5	4.5	5	
			16 MHz	4	4.5	4	4.5	
			8 MHz	3	4	3	4	

[1]External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.

[2]Data based on characterization results, tested in production at VDD max, f_{HCLK} max. and TA max.

[3]Based on characterization, not tested in production.

Maximum current consumptions in Stop and Standby modes (32 KB Flash capacity)

Symbol	Parameter	Conditions	Max				Unit
			Before		After		
			T _A = 85 °C[2]	T _A = 105 °C[1]	T _A =85°C[2]	T _A =105°C[1]	
I _{DD}	Supply current in Stop mode	Regulator in Run mode, low speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	200	370	160	200	μA
		Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	180	340	145	185	
	Supply current in Standby mode[3]	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	3.2	4.5	3.2	4.5	
I _{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.9	2.2[2]	1.9	2.2[2]	

[1]Data based on characterization results, tested in production at V_{DDmax}, f_{HCLK} max. and T_A max.

[2]Based on characterization, not tested in production.

[3]To have the Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} Standby (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).

Typical current consumptions in Stop and Standby modes (32 KB Flash capacity)

Symbol	Parameter	Conditions	Typ[1]				Unit
			Before		After		
			$V_{DD} / V_{BAT} = 2.4V$	$V_{DD} / V_{BAT} = 3.3V$	$V_{DD} / V_{BAT} = 2.4V$	$V_{DD} / V_{BAT} = 3.3V$	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	23.5	24	23.5	24	μA
		Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	13.5	14	13.5	14	
	Supply current in Standby mode[2]	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.7	2	1.7	2	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	1.1	1.4	

[1]Typical values are measured at $T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, unless otherwise specified.

[2]To have the Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} Standby (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).

Part number summary

Old part number	New Part number	Memory size	Package	Line
STM32F103R6T6	STM32F103R6T6A	32K	LQFP64	Performance
STM32F101R6T6	STM32F101R6T6A	32K	LQFP64	Access
STM32F103C6T6	STM32F103C6T6A	32K	LQFP48	Performance
STM32F101C6T6	STM32F101C6T6A	32K	LQFP48	Access
STM32F103T6U6	STM32F103T6U6A	32K	QFN36	Performance
STM32F101T6U6	STM32F101T6U6A	32K	QFN36	Access

Reliability Qualification Plan

New Product Little Piranha

General Information		Locations	
Product Line	<i>CORTEX</i>	Wafer fab location	<i>WF3 / 0.18μm</i>
Product Description	<i>Little Piranha - Die 412</i>	Assembly plant location	<i>Malta- Muar- Carsem</i>
Commercial Product	<i>STM32</i>		
Product division	<i>MMS MCD</i>		
Package Description	<i>TQFP64 - TQFP48 - QFN 36</i>		

The Quality of a product is built-in during the design, material procurement, manufacturing, testing and screening.

The reliability tests are performed to assess the integrity of product subjected to extreme physical and electrical conditions.

They guarantee the product reliability during the end-application manufacturing and operation.

The methodology for product approval will be performed in accordance to STMicroelectronics standard operating procedures (SOP).

1.1 Qualification plan

Qualification type	Derivative product / Derivative NVM
NPR ref	NPR412
Device name	412
Test vehicle	STM32F103
Package	TQFP64 - TQFP48 - QFN 36
Assembly site	MALTA - MUAR - CARSEM
Process type	018MMEMBF/2P5M
Diffusion site	WF3
Test site	Rousset -AngMoKio (EWS) / Malta-Muar (FINAL TEST)

<u>Lot ref:</u>	<u>Qualification type:</u>	<u>Start qual</u>	<u>End qual</u>
	Product		
1	TQFP64 – 12 parts for ESD HBM-CDM/LU TQFP48 – 3 parts for ESD CDM QFN36 – 3 parts for ESD CDM	April 08	May 08
1	TQFP64- 77 Plastic finish good for HTOL168h	June 08	June 08

1.2 Reliability Trials

The following tests will be performed in order to check the reliability performances.

1.2.1 DIE ORIENTED TESTS

TEST	METHOD	CONDITION	Duration Qualification (Monitoring)	Sampling Size / lot
ESD Human Body Model(HBM)	ADCS0060102 JESD22 A114	1500 Ω , 100 pF 2 Kv	NA	3
Charge Device Model(CDM) Latch up (LU)	ADCS 0018695	750V on corner pins, 500V on others T= 105°C	NA	3/ package 6
Early Life Failure Rate (ELFR) High Temperature Operating Life Test (HTOL)=	JESD74 (Q100-008)	140°C, 3.6V	24 hrs/168hrs	77

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