PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM/08/3425
Notification Date 02/18/2008

New location for PDIP 8-14-16L packages in Nantong Fujitsu (CHINA)

APM - APM

Table 1. Change Implementation Schedule

Forecasted implementation date for change	08-May-2008
Forecasted availabillity date of samples for customer	11-Feb-2008
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Feb-2008
Estimated date of changed product first shipment	19-May-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly location change
Reason for change	To improve service and increase our capacity
Description of the change	Following ST commitment towards a continuous improvement of service, it has been decided to increase PDIP 8-14-16 production capacity setting up a new Assembly & Testing location in Nantong Fujitsu (NFME) plant (CHINA). PDIP 8-14L packages are qualified for assembly process for Std Linear Division in NFME, while PDIP16L package is qualified for assembly and testing process for Std Digital Division. Currently, NFME is a ST qualified subcontractor for many other large volume packages. Either the electrical and mechanical characteristics and the level of quality and reliability of product manufactured in NFME are aligned to ST standard. Samples for devices used as Test Vehicles are available.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	"GF" (Assy plant code) as first digits on the label traceability code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	**PCN APM/08/3425**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 02/18/2008**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

....

....

....

....

....

....

....

....

DOCUMENT APPROVAL

Name	Function
Fong, Steven	Division Marketing Manager
Gilot, Yves	Division Marketing Manager
Kaire, Jean-Claude	Division Product Manager
Russo, Biagio	Division Product Manager
Lisi, Giuseppe	Division Q.A. Manager
Paccard, Francoise	Division Q.A. Manager

Reliability Report

On DIP16 - NFME subcontractor – FULL RIVER Frame

General Information	
Product Line	***: P53B***
Product Description	***: TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER***
Commercial Product	***: HCF4053BEY***
Product Group	***: Advanced Analog Logic***
Product Division	***: IMS - APM GROUP***
Package Description	***: DIP 16L***
Silicon Process Technology	***: NHFSFII***

Locations	
Wafer fabrication location	***: ANGMOKIO***
Assembly plant location	***: NFME NANTONG FUJISU***
Final test plant location	***: NFME NANTONG FUJISU***

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
0.1	20-July-07	8	A. Basile G. Presti	Original document

Reliability is the attitude of element to satisfy required function in fixed conditions during established time.

COMPANY CONFIDENTIAL

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW 3
1.1 OBJECTIVES 3
1.2 CONCLUSION 3
2 DEVICE CHARACTERISTICS 3
2.1 DEVICE DESCRIPTION...3
2.2 TRACEABILITY 3
2.2.1 Wafer fabrication information 3
2.2.2 Assembly information 3
3 RELIABILITY TESTS RESULTS 4
3.1 RELIABILITY TEST PLAN AND RESULTS SUMMARY 4
3.2 DIE ORIENTED TESTS(MANDATORY IN CASE OF RELIABILITY EVALUATION RELATED TO DIE)............................6
3.3 PACKAGE ORIENTED TESTS(MANDATORY IN CASE OF RELIABILITY EVALUATION RELATED TO PACKAGE) 6
4 APPLICABLE AND REFERENCE DOCUMENTS...7
5 GLOSSARY 7
6 ANNEXES 8

COMPANY CONFIDENTIAL

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on HCF4053B device in order to qualify DIP14/16 package assembled in NFME subcontractor.

This product is processed in NHSFII technology, diffused in ST ANGMOKIO plant and assembled in DIP16 package using FULL RIVER Lead Frame.

1.2 Conclusion

The final reliability results are positive for all stressed lots.

2 DEVICE CHARACTERISTICS

2.1 Device description

HCF4053B - TRIPLE 2- CHANNEL ANALOG MULTIPLEXER /DEMULTIPLEXER (Datasheet rev. October 2002).
The HCF4053B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor.tecnology available in DIP Package. It is a digitally controlled analog switch having low ON impedance and very low OFF leakage current.

2.2 Traceability

2.2.1 Wafer fabrication information

- Wafer fabrication manufacturing location: ANGMOKIO
- Technology: NHFSII
- Die size: 1.349 X 1.572
- Passivation type: PVAPOX

2.2.2 Assembly information

- Assembly site: NFME (NANTONG FUJITSU)
- Package description: DIP16
- Frame: FULLRIVER
- Wire: Au

COMPANY CONFIDENTIAL

3 RELIABILITY TESTS RESULTS

3.1 Reliability test plan and results summary

Include here the tests plan and the results summary.

Die oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
HTB	High Temperature Bias				
		TA=125℃ Vbias=18V	77x1 Lot	**1000h**	0/77
HTS	High Temperature Storage				
			77x3 Lots	**1000h**	0/231

Package oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
T.H.B.	Temperature Humidity Bias				
		TA=85℃ – RH=85%, Vbias=15V	77x3 Lots	**1000h**	0/231
T.C.	Thermal Cycle				
		TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77x3 Lots	**500cy**	0/231
P.P.	Pressure Pot				
		TA=121℃ – PA=2ATM	77x3 Lots	**168h**	0/231

COMPANY CONFIDENTIAL

LATCH - UP

5.1 Input and Output Injection Latch-up.

TEST CONDITIONS	
TEST ENVIRONMENT	Automated DC Bench
SAMPLE SIZE	4 Devices
TEMPERATURE	+25°C
SUPPLY VOLTAGE	Vcc=5.5V
TEST METHOD	UDCS 0018695

TEST DESCRIPTION

Negative Current Trigger (NIT):
Input and Output pins injected with current sweep from 0mA to -500mA, -50mA steps
Tested output conditions:
1) Active; Output conditioned LOW
2) 3-state mode

Results :
No Latch - up was observed

ESD tests

TEST CONDITIONS Date 23/01/2008	
Type of test	
IMCM System	*Keytek*
Zap Circuit	HBM11-C
Testing Program	manual bench
Failure Criteria	*Functional and electrical Parameters*
Test Method	*JESD22-A115*
Devices	HCF4053
Package	DIP16

Made by: Angelo Castro

Zap Voltage (kV)	n. of Zap	Zap vs Vcc	Zap vs GND	Zap vs I/O pin	Zap +	Zap -	n. of Sample		Results
							Zapped	Failed	
2	1	y	y	y	y	y	3	0	OK

ESD test is SATISFACTORY.

3.2 Die oriented tests

These tests are performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and reverse biased.
The purpose of this test is to detect surface defects such as poor passivation, presence of contaminants, metal corrosion, etc

3.3 Package oriented tests

These tests are performed in order to check device life in various environmental conditions in an accelerated way.
Detectable failure mechanisms are metal corrosion and molding defect, cracking of die, breaking of wire bonding, mechanical damage to the device case.

COMPANY CONFIDENTIAL

4 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
SOP 2610	: General product qualification procedure
Internal ST specification	: Reliability Tests and criteria for qualifications (CORPORATE Q&R RULES)
…	

5 GLOSSARY

ESD	: Electro Static Discharge
LU	: Latch Up

COMPANY CONFIDENTIAL

6 ANNEXES

COMPANY CONFIDENTIAL

Reliability Report

On DIP16 - NFME subcontractor –MHT Frame

General Information	
Product Line	***: P53B***
Product Description	***: TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER***
Commercial Product	***: HCF4053BEY***
Product Group	***: Advanced Analog Logic***
Product Division	***: IMS - APM GROUP***
Package Description	***: DIP 16L***
Silicon Process Technology	***: NHFSFII***

Locations	
Wafer fabrication location	***: ANGMOKIO***
Assembly plant location	***: NFME NANTONG FUJISU***
Final test plant location	***: NFME NANTONG FUJISU***

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
0.1	20-July-07	8	A. Basile G. Presti	Original document

Reliability is the attitude of element to satisfy required function in fixed conditions during established time.

COMPANY CONFIDENTIAL

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW 3
1.1 OBJECTIVES 3
1.2 CONCLUSION 3
2 DEVICE CHARACTERISTICS 3
2.1 DEVICE DESCRIPTION 3
2.2 TRACEABILITY 3
2.2.1 Wafer fabrication information 3
2.2.2 Assembly information 3
3 RELIABILITY TESTS RESULTS 4
3.1 RELIABILITY TEST PLAN AND RESULTS SUMMARY 4
3.2 DIE ORIENTED TESTS(MANDATORY IN CASE OF RELIABILITY EVALUATION RELATED TO DIE) 6
3.3 PACKAGE ORIENTED TESTS(MANDATORY IN CASE OF RELIABILITY EVALUATION RELATED TO PACKAGE) 6
4 APPLICABLE AND REFERENCE DOCUMENTS 7
5 GLOSSARY 7
6 ANNEXES 8

COMPANY CONFIDENTIAL

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on HCF4053B device in order to qualify DIP14/16 package assembled in NFME subcontractor.

This product is processed in NHSFII technology, diffused in ST ANGMOKIO plant and assembled in DIP16 package using FULL RIVER Lead Frame.

1.2 Conclusion

The final reliability results are positive for all stressed lots.

2 DEVICE CHARACTERISTICS

2.1 Device description

HCF4053B - TRIPLE 2- CHANNEL ANALOG MULTIPLEXER /DEMULTIPLEXER (Datasheet rev. October 2002).
The HCF4053B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor.tecnology available in DIP Package. It is a digitally controlled analog switch having low ON impedance and very low OFF leakage current.

2.2 Traceability

2.2.1 Wafer fabrication information

- Wafer fabrication manufacturing location: ANGMOKIO
- Technology: NHFSII
- Die size: 1.349 X 1.572
- Passivation type: PVAPOX

2.2.2 Assembly information

- Assembly site: NFME (NANTONG FUJITSU)
- Package description: DIP16
- Frame: MHT
- Wire: Au

COMPANY CONFIDENTIAL

3 RELIABILITY TESTS RESULTS

3.1 Reliability test plan and results summary

Include here the tests plan and the results summary.

Die oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
HTB	High Temperature Bias				
		TA=125℃ Vbias=18V	77x1 Lot	**1000h**	0/77
HTS	High Temperature Storage				
			77x3 Lots	**1000h**	0/231

Package oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
T.H.B.	Temperature Humidity Bias				
		TA=85℃ – RH=85%, Vbias=15V	77x3 Lots	**1000h**	0/231
T.C.	Thermal Cycle				
		TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77x3 Lots	**500cy**	0/231
P.P.	Pressure Pot				
		TA=121℃ – PA=2ATM	77x3 Lots	**168h**	0/231

COMPANY CONFIDENTIAL

LATCH - UP

5.1 Input and Output Injection Latch-up.

TEST CONDITIONS	
TEST ENVIRONMENT	Automated DC Bench
SAMPLE SIZE	4 Devices
TEMPERATURE	+25°C
SUPPLY VOLTAGE	Vcc=5.5V
TEST METHOD	UDCS 0018695

TEST DESCRIPTION

Negative Current Trigger (NIT):
Input and Output pins injected with current sweep from 0mA to -500mA, -50mA steps
Tested output conditions:
1) Active; Output conditioned LOW
2) 3-state mode

Results :
No Latch - up was observed

ESD tests

TEST CONDITIONS Date 23/01/2008	
Type of test	
IMCM System	*Keytek*
Zap Circuit	HBM11-C
Testing Program	manual bench
Failure Criteria	*Functional and electrical Parameters*
Test Method	*JESD22-A115*
Devices	HCF4053
Package	DIP16

Made by: Angelo Castro

Zap Voltage (kV)	n. of Zap	Zap vs Vcc	Zap vs GND	Zap vs I/O pin	Zap +	Zap -	n. of Sample		Results
							Zapped	Failed	
2	1	y	y	y	y	y	3	0	OK

ESD test is SATISFACTORY.

3.2 Die oriented tests

These tests are performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and reverse biased.
The purpose of this test is to detect surface defects such as poor passivation, presence of contaminants, metal corrosion, etc

3.3 Package oriented tests

These tests are performed in order to check device life in various environmental conditions in an accelerated way.
Detectable failure mechanisms are metal corrosion and molding defect, cracking of die, breaking of wire bonding, mechanical damage to the device case.

COMPANY CONFIDENTIAL

4 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
SOP 2610	: General product qualification procedure
Internal ST specification	: Reliability Tests and criteria for qualifications (CORPORATE Q&R RULES)
…	

5 GLOSSARY

ESD : Electro Static Discharge
LU : Latch Up

COMPANY CONFIDENTIAL

6 ANNEXES

COMPANY CONFIDENTIAL

Reliability Report

Assembly qualification

General Information	
Product Line	*: 0393*
Product Description	*: Dual comparator*
Commercial Product	*: LM393N*
Product Group	*: APM*
Product Division	*: Standard IC's*
Package Description	*: Minidip 8*
Silicon Process Technology	*: Bipolar*

Locations	
Wafer fabrication location	*: Ang Mo Kio*
Assembly plant location	*: Nantong Fujitsu China*
Final test plant location	*: ST Shenzhen China*

General Information	
Product Line	*: 0124*
Product Description	*: Dual Operational amplifier*
Commercial Product	*: LM324N*
Product Group	*: APM*
Product Division	*: Standard IC's*
Package Description	*: DIP14*
Silicon Process Technology	*: Bipolar*

Locations	
Wafer fabrication location	*: Ang Mo Kio*
Assembly plant location	*: Nantong Fujitsu China*
Final test plant location	*: ST Shenzhen China*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
0.1	24-Jan-07	5	JM Bugnard	Original document

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW....3
1.1 OBJECTIVES....3
1.2 CONCLUSION....3
2 DEVICE CHARACTERISTICS....3
2.1 DEVICE DESCRIPTION....3
2.2 TRACEABILITY.... ERROR! BOOKMARK NOT DEFINED.
2.2.1 Assembly information
Error! Bookmark not defined.
3 RELIABILITY TESTS RESULTS....4
3.1 RELIABILITY TEST PLAN AND RESULTS SUMMARY....4
4 APPLICABLE AND REFERENCE DOCUMENTS....5
5 GLOSSARY....5

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

This Qualification Report summarizes the reliability trials and results performed to qualify the DIP package, Nantong Fujitsu China assembly line.
This document is the official report of the qualification of the DIP package Nantong Fujitsu China assembly plant for standard linear Ic's.
The test conditions and results are presented in chapter 3.

1.2 Conclusion

Based on reliability results and construction analysis results, DIP8 and 14 leads assembled in Nantong Fujitsu China are qualified for standard linear IC's

2 DEVICE CHARACTERISTICS

2.1 Device description

	TV1	TV2
Line	0393	0124
Sales Type	LM393N	LM324N
Diffusion site	Ang Mo Kio Singapore	
FE process	Bipolar	Bipolar
Package	DIP8	DIP14
Die size (µm)	950 X 870 µm	1430 X 1360 µm
Die thickness (µm)	280µm	280µm
Metallization	AlSiCu	AlSiCu
Passivation	Nitride	Nitride
Back side	Raw silicon	Raw silicon

2.2 TRACEABILITY

2.2.1 Assembly information

	New
Assembly location	Nantong-Fujitsu China
Die attach	YiI HUA 9005SP-2
Wire	Gold 1 Mils
Leadframe	Copper 80x80 mils for DIP14 100x100mils for DIP8
Molding compound	HYSOL HUA WEI KLA4000-1T
Lead finishing	Sn plating

3 RELIABILITY TESTS RESULTS

Include here a general description of the reliability evaluation strategy. If the test plan is not in line with the one planned initially, include necessary explanation.

3.1 Reliability test plan and results summary

Die oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
HTB	LM393N				
		Tamb= 150℃ , Vcc=+/-15V	78	1000h	0/78
HTB	LM324N				
		Tamb= 150℃ , Vcc=+/-15V	78	1000h	0/78

Package oriented test

Test	Test short description				
	Method	Conditions	Sample Size	Duration	Results Fail/ Sample Size
THB	LM393N				
	JEDEC JESD22 A101	Tamb.: 85℃, Rel. Humidity: 85%, Vcc: +/- 15V	78	1000h	0/78
THB	LM324N				
	JEDEC JESD22 A101	Tamb.: 85℃, Rel. Humidity: 85%, Vcc: +/- 15V	78	1000h	0/78
PPT	LM393N				
	JEDEC JESD22 A102	T°amb.:121℃, Presure: 2 atm	54	240h	0/54
TMC	LM393N				
	JEDEC JESD22 A104C	T°amb.:-65/+150℃ (2 cycles per hour) air to air	78	1000cy	0/78
TMC	LM324N				
	JEDEC JESD22 A104C	T°amb.:-65/+150℃ (2 cycles per hour) air to air	78	1000cy	0/78

Conclusion: Based on these results and on construction analysis performed on these packages, DIP package is qualified for standard linear Ic's in Nantong Fujitsu (China).

4 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
SOP 2610	: General product qualification procedure

5 GLOSSARY

PC	: Preconditioning
ESD	: Electro Static Discharge
HTB	: High Temperature Bias
THB	: Temperature and Humidity Bias
PPT	: Pressure Pot
TMC	: Thermal Cycling

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS ‘‘AUTOMOTIVE GRADE’’ MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

© 2008 STMicroelectronics - All rights reserved.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morroco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com