



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-DIS/08/3312
Notification Date 01/31/2008

APM - ASD & IPAD Division
Thyristors in Top Glass technology
Die layout optimisation
DIS - ASD & IPAD

Table 1. Change Implementation Schedule

Forecasted implementation date for change	31-Jan-2008
Forecasted availability date of samples for customer	24-Jan-2008
Forecasted date for STMicroelectronics change Qualification Plan results availability	24-Jan-2008
Estimated date of changed product first shipment	01-May-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	All Triacs & SCRs in Top Glass technology
Type of change	Product design change
Reason for change	Production process optimisation
Description of the change	The die periphery is optimised with our last technology development, the mesa groove being resized according to our design rules.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Internal codification and QA number
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Paris, Eric	Division Marketing Manager
Duclos, Franck	Division Product Manager
Besson, Andre	Division Q.A. Manager

WHY THIS CHANGE?

The permanent evolution of our technology leads us to implement a new **die layout optimization** for our **SCRs** and **Triacs** in **Top Glass Technology**. This change ensures full optimisation of our production process.

The involved product series are listed in the table below:

Product Sub-Family	Product PN or Series	Package
SCRs	TNxxx-xxxB(-TR) / H TSxxx-xxxB(-TR) / H TSxxx-xxxH / T TYN612MRG / FP X02xxx X04xxx X006xxx JTT04/ JTTL04-xxx	DPAK / IPAK DPAK / IPAK IPAK / TO-220AB TO-220AB / TO-220FPAB SOT-223 / TO-92 TO-202-1 /-3 SOT-223 / TO-92 Wafer form
TRIACs	BTB04-600SL Txxx-xxxB(-TR) / H Z01xxx Z04xxx Z006xxx JCTW08-xxx	TO-220AB DPAK / IPAK SOT-223 / TO-92 TO-202-1 /-202-3 SOT-223 / TO-92 Wafer form

Specific Thyristors manufactured by ST in the Top Glass technology, even if not expressly included in the above table, are affected by this change.

WHAT IS THE CHANGE?

The **die periphery** is optimised with our last technology development, meaning with the mesa groove **resized** according to our design rules.

The **active area** remains exactly the **same** as for current versions, resulting in rigorously the same electrical parameters and performance for all products, with respect to the product datasheet.

The verification by characterization that there is **no impact on the electrical parameters**, including the **leakage current** (I_{DRM}/I_{RRM}), the **non-repetitive surge peak on-state current** (I_{TSM}) and the **peak on-state voltage drop** (V_{TM}), is included in the qualification program.

HOW AND WHEN?Qualification program and results availability:

The **qualification program** mainly consists of **comparative electrical characterizations** and **reliability tests**.

This **qualification program** is provided in appendix 1 to this document. The **reliability test report** and the **characterization report** of the qualification program are available on request **now**.

Samples availability:

Samples of selected devices, including test vehicles used for qualification, are **available** on request as indicated below:

Salestypes	Product Sub-Family	Availability
TS450-600B TS820-800B X00605MA	SCRs	NOW
BTB04-600SL T405-600B/H T410-800B/T Z00607MA Z0103MN/NA Z0109SN	TRIACs	NOW

Other samples are available on request for delivery within notice period if ordered within 30 days.

Change implementation schedule:

The **production start** and **first shipments** will be implemented according to our work in progress and materials availability as indicated in the schedule below:

Production Start	1st Shipments
From Week 05-2008	From Week 18-2007

Lack of acknowledgement of the PCN within **30 days** will constitute acceptance of the change. After acknowledgement, lack of additional response within the **90 day** period will constitute acceptance of the change (Jedec Standard JESD46C). In any case, **first shipments** may start earlier with customer's **written agreement**.

Marking and traceability:

The **traceability** for the new die layout will be ensured by an **internal codification** and by the **Q.A. number**.

Appendix 1: Reliability tests for qualification program.



Thyristors in Top Glass technology: Die layout optimisation

Reliability tests for QUALIFICATION

Test vehicles	Description	Package
BTB04-600SL	Std Triac 4A 600V 10 mA Lighting	TO-220AB
T410-600B	Snubberless Triac 4A 600V 10 mA	DKPAK
Z00607MA 1BA2	Standard Triac 0.8A 600V 5 mA	TO-92

QUALIFICATION TESTS					
TEST	CONDITIONS	DURATION	NBR OF LOTS (*)	SAMPLE SIZE	ACCEPTANCE CRITERIA
Parametric verification vs datasheet + distribution comparison	See datasheet	-	3	25 pcs / lot	Datasheet
Thermal Cycling JESD22-A104	-55°C/+150°C Air/Air	1000 cycles	1	77 pcs / lot	0 failure
High Temperature Reverse Bias JESD22 A-108	Vbias = 600Vac Tamb = 125°C	1000 hours	3	77 pcs / lot	0 failure

(*) Lots selected among test vehicles of the list above or of other devices presenting sufficient technological similarities.
NOTE: A preconditioning sequence is performed on SMD products before TC reliability tests according to JESD22-A113.

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