PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/07/3302
Notification Date 12/26/2007

M95256, 256Kbit Serial SPI Bus EEPROM Upgrade and Die Optimization

MMY - MEMORY

Table 1. Change Implementation Schedule

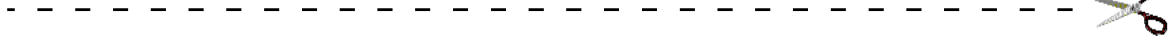
Forecasted implementation date for change	04-Jan-2008
Forecasted availabillity date of samples for customer	18-Jan-2008
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	18-Jan-2008
Estimated date of changed product first shipment	26-Mar-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M95256 products family
Type of change	Product design change
Reason for change	Increase performance
Description of the change	Metal 1 mask
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process and fab ID see marking above
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/07/3302**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 12/26/2007**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Division Marketing Manager
Rodrigues, Benoit	Division Product Manager
Yackowlew, Nicolas	Division Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

M95256, 256Kbit Serial SPI Bus EEPROM
Upgrade and Die Optimization

What is the change?
The M95256, 256Kbit Serial SPI Bus EEPROM product family, will undergo a design change: a metal 1 mask change will allow a better trimming of the programming voltage, it will improve the product programmability and endurance over the full Automotive grade temperature (-40°C / 150°C).
As part of ST commitment to continuous improvement, this design change will be implemented for the whole production.

Why?
The strategy of STMicroelectronics Memory Division is to support the growth of our customers on a long-term basis. In line with this commitment, the qualification of the redesigned M95256 will allow to serve new markets requiring high endurance at high temperature as well as applications in industrial range with a single product design.

When?
The production of the upgraded M95256 in the ST Rousset (France) 8 inch wafer diffusion plant will ramp up from January 2008 and shipments will start from March 2008 onward.

How will the change be qualified?
The new version of the M95256 will be qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.
The qualification report QREE0522 will be updated (rev 06) and will be available on Week 03 / 2008.
Note: a similar design solution was already qualified in the M95512 from same process.

What is the impact of the change?

- **Form:** marking change (see **Device marking** paragraph)

- **Fit:** no change

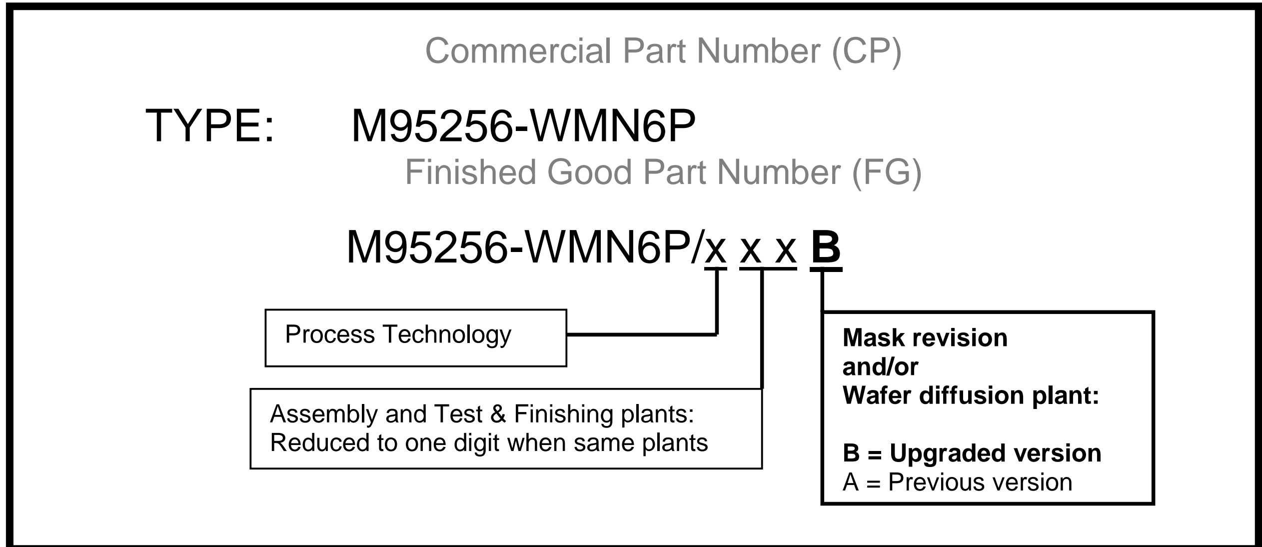
- **Function:** Higher endurance over the full Automotive grade temperature range (-40°C / 150°C).
The Datasheet remains identical.

How can the change be seen?

- BOX LABEL MARKING

On the BOX LABEL MARKING, the change is visible inside the Finished Good Part Number: the **Mask revision and /or Wafer diffusion plant** identifier is “**B**” for the **upgraded version in SO8N**, this identifier being “A” for the previous version.

➔ *Example for M95256-WMN6P (2.5V to 5.5V Vcc range, SO8N RoHS* compliant package)*



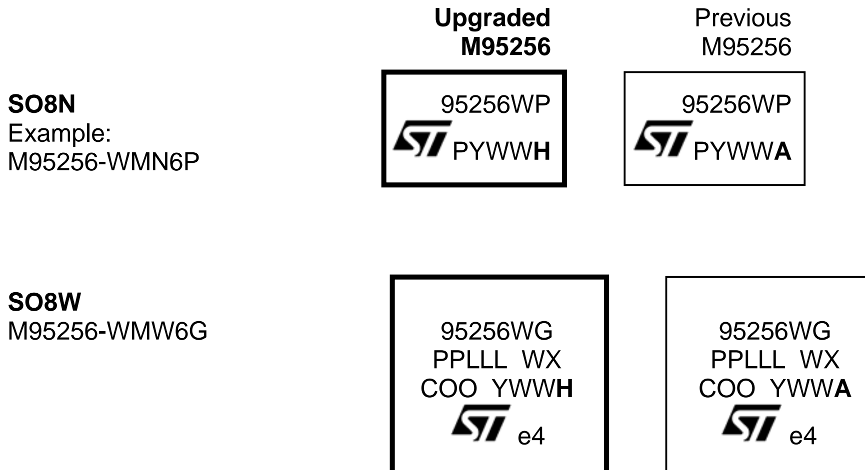
*RoHS: Restriction of the use of certain Hazardous Substances in electrical and electronic equipments

How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the **SO8N** package, the change is visible inside the trace code (PYWWT) where the last digit “T” for **Process Technology** identifier is “**H**” for the **upgraded version**, the identifier being “A” for the previous version.

On the DEVICE MARKING of the **SO8W**, the change is visible inside the second line of the trace code (YWWT) where the last digit “T” for **Process Technology** identifier is “**H**” for the **upgraded version**, the identifier being “A” for the previous version.



The traceability for each device is as follows:

P or PP Y WW LLL WX T

P(PP) = Assembly country & plant
Y = Last digit of the Year of Assembly
WW = Assembly Week code
LLL = chronological sequence
WX = Wafer diffusion plant
COO = Country of origin (Assembly)
T = Process Technology code/ Wafer Fab ID

For **TSSOP8** package size reason, the change is not visible on the device marking. The change is only visible inside the Finished Good Part Number appearing on the BOX LABEL MARKING (see previous page).

Appendix A- Product Change Information

Product family / Commercial products:	M95256 products family
Customer(s):	All
Type of change:	Design refine
Reason for the change:	Increase performance
Description of the change:	Metal 1 mask
Forecast date of the change:	January 2008
Forecast availability date of qualification sample for the customer(s):	Week 03 / 2008
Forecast date for the internal STMicroelectronics change, Qualification report availability:	Week 03 / 2008
Marking to identify the changed product:	Process and fab ID see marking above
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See list of concerned products in appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	March 2008
Division Product Manager: B. RODRIGUES	Date:
Group QA Manager: N. YACKOWLEW	Date:

Appendix B: concerned products:

M95256-WMN6P
M95256-WMN6TP
M95256-WDW6TP
M95256-WMW6G
M95256-WMW6TG
M95256-RMN6P
M95256-RMN6TP
M95256-RDW6TP

Appendix C: Qualification Plan:

M95256 Redesigned version B

Using **CMOSF8L** silicon process technology in **R8** Fab

PRODUCT DESCRIPTION

	Device to qualify	Qualified similar device
Product name	M95256 Redesigned version B	*M95512 / M24512*
Memory size	256K	512K
Bus protocol	SPI	SPI
Process	CMOSF8L / R8	CMSOF8L / R8

SIMILARITY

The new metal mask was already qualified on the 512K SPI and I2C products (respectively QREE0703 and QREE0719).
According to STMicroelectronics specifications 0068577 and SOP2.6.14, the qualification activities were planned on 1 lot for die-oriented trials.

CHARACTERIZATION

Table 1. Characterization requirements.

Number of lots	Parameters	Vcc range	Temperature range
1	All	1.8V/5.5V	-40°C/150°C

RELIABILITY TEST PLAN

Table 2. Die-oriented reliability test plan and results summary

Test	Test short description					
	Method	Conditions	Sample size / lots	Number of lots	Duration	Results fail / sample size
EDR (HTOL after W/E)	High temperature operating life after endurance					
	AEC-Q100-005 JESD22-A108	1Mcy W/E @ 25°C then: HTOL 150°C / 1.2xVcc max (6V)	80	1	1008 hours	0/80
EDR (Bake after W/E)	Data retention after endurance					
	AEC-Q100-005 JESD22-A103	1Mcy W/E @ 25°C then: Retention Bake at 150°C Retention field = Checkerboard	80	1	1008 hours	0/80
LTOL	Low temperature operating life					
	JEDEC JESD22-A108	-40°C / 1.2xVcc max (6V)	80	1	1008 hours	0/80
HTSL	High temperature storage life					
	AEC-Q100-005 JESD22-A103	200°C / No bias Retention field = Checkerboard	80	1	1008 hours	0/80
WEB	Program/Erase endurance cycling + bake					
	Internal spec.	Cycling at 25°C / Vcc max then: Retention Bake at 200°C / 48 hours Retention field = Checkerboard	80	1	1000Kcycles / 48 hours	0/80 (1)
ESD (HBM)	Electro static discharge (human body model)					
	AEC-Q100-002 JESD22-A114	C = 100 pF, R = 1500 Ohms	27	1	N/A	Pass > 4000V
ESD (MM)	Electro static discharge (machine model)					
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ohms	9	1	N/A	Pass > 400V
LU	Latch-up (current injection and overvoltage stress)					
	AEC-Q100-004 JESD78A	At maximum operating temerature (150°C)	6	1	N/A	Class II - Level A

1. First rejects after 10 million cycles + Bake.

Document Revision History

Date	Rev.	Description of the Revision
Oct. 01, 2007	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

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