PRODUCT/PROCESS CHANGE NOTIFICATION

PCN HED-AUD/08/2897
Notification Date 01/21/2008

NEW MOLDING COMPOUND INTRODUCTION FOR SSOP IN AMKOR ATP1

AUD - AUDIO

Table 1. Change Implementation Schedule

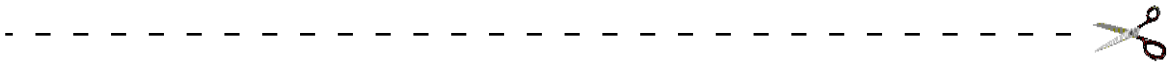
Forecasted implementation date for change	14-Apr-2008
Forecasted availabillity date of samples for customer	14-Jan-2008
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	14-Jan-2008
Estimated date of changed product first shipment	21-Apr-2008

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	TDA7469 and TDA746913TR
Type of change	Package assembly material change
Reason for change	Molding compound material change
Description of the change	Following a Company package roadmap, we are on going to introduce the molding compound SUMITOMO G600 on SSOP line assembled in Amkor ATP1 Philippines subcontractor plant. Qualification Certificate (QC-95-06-C) available upon request.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Internal sales type change only
Manufacturing Location(s)	1]Sc Amkor Atp1 - Philippines

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN HED-AUD/08/2897**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 01/21/2008**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Onetti, Andrea Mario	Division Marketing Manager
Angelici, Marco	Division Product Manager
Piccoli, Massimo	Division Q.A. Manager

MOLDING COMPOUND SUMITOMO G600 INTRODUCTION ON SSOP PACKAGE IN AMKOR ATP1

WHAT:
Following a Company package roadmap, we are on going to introduce the molding compound SUMITOMO G600 on SSOP line Pure Tin assembled in AMKOR ATP1 Philippines subcontractor plant.
This molding compound already used in AMKOR ATP1 on SO28 line.

Audio product affected by this change is :

Line	Sales Type	Package
A769	TDA7469 & TDA746913TR	SSOP24

WHY:
Company package strategy for SO and SSOP packages.

HOW:
Reliability Report HPC-Rel-33-06-B on SO28 package and positive workability test on SSOP package, cover the change involved in this PCN.

WHEN:
From April 07 deliveries onward.

HED BE Q&R RELIABILITY REPORT*

Assembly line: SO line Pure Tin – AMKOR-ATP1
Package family: SO28 (LR package code)

Abstract

The object of this reliability report is to validate the introduction of the pure tin finishing and the molding compound (G600) change.

Change identification

Reliability report reference / date	HPC-Rel-33-06-B	June 5, 2007
Qualification request reference /date	HPC 0063/05	December 7, 2005
Qualification plan reference / date	HPC QP06010	April 25, 2006
Affected products	SO 28 lead free	

Conclusion

Based on the results of reliability tests and TI, all SO 28 with pure tin finishing can be considered as qualified with JEDEC level 3 @260°C (peak reflow temperature).

* HED BE Q&R – GRENOBLE
Issued by Corinne TRIOMPHE
Approved by Massimo PICCOLI

Package construction note

PACKAGE FEATURES	
Package name	SO 28 .30 TO JEDEC MS-013AE
Body size (mm^3)	18 x 7.5 x 2.3
Pitch (mm)	1.27
Assembly site	AMKOR ATP1
Lead finish	Pure Tin
Solder plating machine	MECO
Solder plating chemistry	EXCEL 90
Die attach	Ablestik 8290
Molding compound	Resin Sumitomo G600
Wire material / diameter	GOLD WIRE 1.2 MILS DIAM.
Wire bonding	Thermosonic

Test vehicles definition

DIE & PRODUCT FEATURES			
Technical code/ Line	A563	A521	A207
RL Code	D5LR*A563BAZ	ECLR*A521ABQ	B5LR*A207BAH
Pad size (µm²)	3810 x 3810	3810 x 3810	3810 x 3810
Ground wires	No	No	No
Diffusion process	B3 HF2CMOS	B3 HF2CMOS	B3 HF2CMOS
Diffusion plant	Carrolton non HP	Carrolton non HP	Carrolton non HP
Wafer diameter	6”	6”	6”
Wafer thickness (µm)	375	375	375
Die size (µm²)	2840 x 2250	2680 x 2310	3140 x 3030
Die front finishing	P-VAPOX(SiO2) / NITR	P-VAPOX(SiO2) / NITR	P-VAPOX(SiO2) / NITR
Die back finishing	RAW SILICON	RAW SILICON	RAW SILICON

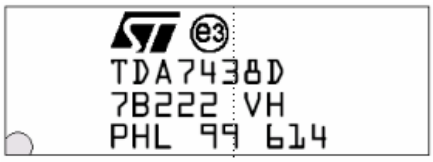
Construction analysis

See Construction analysis report N° CA MALTA HPC38/06, HPC39/06, HPC40/06 – CTLib numbers 27565, 27566, 27567 – Written by Clifford CALLUS (October 10, 2006).

Lot traceability

A563 lot

Assy lot number: H6073850=1
Wafer lot number: VH607385



521 lot

Assy lot number: H606318=1
Wafer lot number: VH606318

A207 lot

Assy lot number: H547469=1
Wafer lot number: VH547469

Reliability test conditions and results

Line	Final test	Reliability plant	Particular points
A563	MUAR	MUAR	
A521	MUAR	MUAR	
A207	MUAR	MUAR	

		REJECTED PARTS		
TEST	**CONDITIONS**	*A563*	*A521*	*A207*
JL3	Preconditioning - T-SCAN + C-SAM @ time 0 - 24h bake @ 125°C - 192h @ 30°C / 60% RH - Reflow simulation (3 times) with standard JEDEC profile @ 260°C - T-SAM + C-SAM after reflow	*0/150*	*0/150*	*0/150*
JL3 + HdTS	Humidity storage Ta=85°C/85%Rh Steps: 0, 168, 500, 1000 hours T-SCAN + C-SAM after 1000 hours	*0/50*	*0/50*	*0/50*
JL3 + TCT	Thermal cycling Ta=-40/+150°C Steps: 0, 100, 500, 1000 cycles T-SCAN + C-SAM after 1000 cycles	*0/50*	*0/50*	*0/50*
HTS	High temperature storage Ta=150°C Steps: 0, 168, 500, 1000 hours T-SCAN + C-SAM after 1000 hours	*0/50*	*0/50*	*0/50*
JL3 + PPT	Pressure pot P=2atm, Ta=121°C, 100%RH Steps: 0, 168, 240h T-SCAN + C-SAM after 240h	*0/50*	*0/50*	*0/50*

Delamination issues on A521 lot

Resin-Lead delamination observed on 1/10 samples of A521 lot in construction analysis.

Initial traces of bottom pad delamination were found on parts n°11, 20 & 21 of A521 lot.
After the JL3 step, this delamination extends to 100% of the die pad (bottom) for the same 3 parts.
After HdTS, part n°21 presents 100% of the die pad (bottom) delamination.
After TCT, all parts present 50 to 100% of the die pad (bottom) delamination.
After PPT, part n°6 presents 100% of the die pad (bottom) delamination.

A Temporary Instruction (TIHPC06-44-A) was put in place to monitor this issue: on all the production, sample 2 strips per assembly lots and perform SAM (top & bottom) during 3 months.
All results of this TI are ok.

Annex: Reliability tests description

TEST NAME	DESCRIPTION	PURPOSE
JLn: JEDEC Level n surface mounting simulation	The device is submitted to a typical temperature profile used for surface mounting, after controlled moisture absorption.	*As stand-alone test:* to investigate the level of moisture sensitivity. *As preconditioning before other reliability tests:* to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TCT: Temperature Cycles Test	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, and die attach layer degradation.
PPT: Pressure Pot Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTS: High Temperature Storage	The device is stored in unbiased condition at the max. Temperature allowed by the package materials, sometimes higher than the max. Operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress voiding.
HdST: Humid Storage Test	The device is stored at controlled conditions of temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by wet conditions. Typical failure mechanisms are corrosion and surface effects related to the molding compound.