PRODUCT/PROCESS CHANGE NOTIFICATION

CMOSM6X-F & CMOSM6D-F PROCESS TECHNOLOGY TRANSFER TO CHARTERED

MIC - MICROCONTROLLERS

Table 1. Change Identification

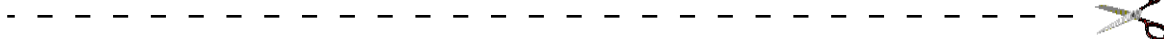|	
Product Identification (Product Family/Commercial Product)	See page 5
Type of change	Waferfab location change
Reason for change	Increased market demand and need for improved production flexibility
Description of the change	Add Chartered fab (Singapore) as a qualified wafer fab. All datasheet parameters are identical to Phoenix silicon.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Package marking from "VP" to "F2"
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

Forecasted implementation date for change	01-Dec-2007
Forecasted availabillity date of samples for customer	01-Dec-2007
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	01-Dec-2007
Estimated date of changed product first shipment	01-Dec-2007

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

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Customer Acknowledgement of Receipt	**PCN MMS-MIC/07/2671**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 06/22/2007**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Benmokhtar, Youssef B	Division Marketing Manager
Nicholas, Jimmy Edward	Division Product Manager
De mingo, Francisco	Division Q.A. Manager

Impacted Part Number		
ST72F260G1B5	ST7FLIT19BF1B6	ST7FLITES2YM6TR
ST72F260G1M6	ST7FLIT19BF1B6EE	ST7FLITES5Y0B6
ST72F260G1M6/TR	ST7FLIT19BF1M3	ST7FLITES5Y0M6
ST72F262G1B5	ST7FLIT19BF1M6	ST7FLITES5Y0M6TR
ST72F262G1B6	ST7FLIT19BF1U6	ST7FLITEU02M6
ST72F262G1M6	ST7FLIT19BY0B6	ST7FLITEU05M6
ST72F262G1M6TR	ST7FLIT19BY0M6	ST7FLITEU09M3
ST72F262G2B5	ST7FLIT19BY1B6	ST7FLITEU09M6
ST72F262G2B6	ST7FLIT19BY1M3	ST7FLITEUS2B3
ST72F262G2M6	ST7FLIT19BY1M6	ST7FLITEUS2B6
ST72F262G2M6TR	ST7FLIT19F1M6TR	ST7FLITEUS2M3
ST72F264G1B5	ST7FLIT19F1M7TR	ST7FLITEUS2M3TR
ST72F264G1M6	ST7FLITE02Y0B6	ST7FLITEUS2M6
ST72F264G2B5	ST7FLITE02Y0M6	ST7FLITEUS2M6TR
ST72F264G2B6	ST7FLITE05DIE70	ST7FLITEUS2U3TR
ST72F264G2H1	ST7FLITE05M6TR	ST7FLITEUS2U6TR
ST72F264G2H1E	ST7FLITE05Y0B6	ST7FLITEUS5B6
ST72F264G2H6	ST7FLITE05Y0M6	ST7FLITEUS5B6EE
ST72F264G2H6E	ST7FLITE09M6TR	ST7FLITEUS5M3
ST72F264G2H6ETR	ST7FLITE09Y0B6	ST7FLITEUS5M3TR
ST72F264G2M6	ST7FLITE09Y0M6	ST7FLITEUS5M6
ST72F264G2M6/TR	ST7FLITE0HY0M6	ST7FLITEUS5M6TR
ST72F561K6T6	ST7FLITE10F1M6	ST7FLITEUS5U3TR
ST72P262M6/NAZTR	ST7FLITE15F1B6	ST7FLITEUS5U6TR
ST72P262M6/NNOTR	ST7FLITE15F1M6	ST7FLITEUSNM3
ST72P264H1/NYZTR	ST7FLITE15M6TR	ST7FMC1K2T6/TR
ST72P264H1NYZTRE	ST7FLITE19F1B6	ST7FMC2R7T6
ST7FDALIF2M6	ST7FLITE19F1M6	ST7LNB0V2Y0M6
ST7FDALIF2M6TR	ST7FLITE20F1B6	ST7LNB0V2Y0M6TR
ST7FLI19BF1M3TR	ST7FLITE20F2B6	ST7LNB0V3Y0M6
ST7FLI19BY1M3TR	ST7FLITE20F2M6	ST7LNB0V3Y0M6TR
ST7FLIT10BF0B6	ST7FLITE25F1B6	ST7LNB0Y0M6
ST7FLIT10BF0M6	ST7FLITE25F2B6	ST7LNB0Y0M6TR
ST7FLIT10BF1B6	ST7FLITE25F2M6	ST7LNB1M6/NAMTR
ST7FLIT10BF1M6	ST7FLITE25M6TR	ST7LNB1Y0M6
ST7FLIT10BY0B6	ST7FLITE29F1B6	ST7LNB1Y0M6/TR
ST7FLIT10BY0M6	ST7FLITE29F2B6	ST7OS15BF1M7
ST7FLIT10BY1B6	ST7FLITE29F2M6	ST7OS15BF1M7/TR
ST7FLIT10BY1M6	ST7FLITE29F2M6TR	ST7PLITE05MSKTR
ST7FLIT15BF0B6	ST7FLITE29F2M7TR	ST7PLITE05NOBTR
ST7FLIT15BF0M3	ST7FLITE30F2B6	ST7PLITE05/OBNTR
ST7FLIT15BF0M6	ST7FLITE30F2M6	ST7PLITE05OBXTR
ST7FLIT15BF1B6	ST7FLITE35F2B6	ST7PLITE05OJZTR
ST7FLIT15BF1M3	ST7FLITE35F2M3	ST7PLITE05OMITR
ST7FLIT15BF1M6	ST7FLITE35F2M6	ST7PLITE05OMJTR
ST7FLIT15BM6TR	ST7FLITE35M6TR	ST7PLITE05OMKTR
ST7FLIT15BY0B6	ST7FLITE35U6TR	ST7PLITE09MBRTR
ST7FLIT15BY0M3	ST7FLITE39F2B6	ST7PLITE09OBMTR
ST7FLIT15BY0M6	ST7FLITE39F2M3	ST7PLITE29MYB/TR
ST7FLIT15BY1B6	ST7FLITE39F2M6	ST7PLITEBC/OFXTR
ST7FLIT15BY1M6	ST7FLITE39F2U6	ST7PLITEBC/OFYTR
ST7FLIT15Y1M6TR	ST7FLITE39M6TR	ST7PLITES2/OKETR
ST7FLIT19BF0B6	ST7FLITEBCY0M6	ST7PLITES5/MLCTR
ST7FLIT19BF0M3	ST7FLITES2Y0B6	ST7PLITES5OIHTR
ST7FLIT19BF0M6	ST7FLITES2Y0M6	

CMOSM6X-F & CMOSM6D-F TRANSFER TO CHARTERED

RELIABILITY PLAN

June 5th, 2007 V1.1

STMicroelectronics

CMOSM6X-F & CMOSM6D-F PRODUCT VEHICLES

**2 TEST VEHICLES WILL ALLOW TO QUALIFY
CMOSM6X-F & CMOSM6D-F PROCESS IN CHARTERED**

	CMOSM6X-F	CMOSM6D-F
TEST VEHICLE	ST7FLITE0	ST7FLITE3
DIE NAME	P819	P852
PACKAGE ASSEMBLY SITE	SO16 MUAR	SO20 MUAR
QUALIFICATION LOTS	1 LOT	2 LOTS
RELIABILITY DURATION	10 weeks (1)	10 weeks (1)

(1)   + 4 weeks for EWS, Assy and FT

CMOSM6X/D-F – RELIABILITY PLAN (1/3)

DIE ORIENTED RELIABILITY TRIALS

TEST	SPECIFICATIONS	NUMBER OF PARTS	ACCEPTANCE CRITERIA
ESD (Human Body Model)	AEC Q100 Method 002	1 LOT 6 PARTS	1500 Ω, 100 pF 2000 V / All leakage < |1 µA|
ESD (Charge Device Model)	AEC Q100 Method 003	1 LOT 6 PARTS	0 Ω, 200 pF 500 V / All leakage < |1 µA|
LATCH UP	AEC Q100 Method 004	1 LOT 6 PARTS	Overstress limits at 1.5 x VDDmax or |100 mA| @ 125°C
DYNAMIC LATCH UP	ADCS 7053449	1 LOT 3 PARTS	330 Ω, 150 pF 1000 V / All leakage < |1 µA|

CMOSM6X/D-F – RELIABILITY PLAN (2/3)

DIE ORIENTED RELIABILITY TRIALS

TEST	SPECIFICATIONS	NUMBER OF PARTS			ACCEPTANCE CRITERIA
		LOT 1	LOT 2	LOT 3	
EARLY FAILURE RATE (1)	AEC Q100 Method 008	500	500	500	24 HRS / 140°C / 6V No reject with std Final Test
HIGH TEMPERATURE OPERATING LIFE TEST (1)	MIL Std 883E Method 1005	77	77	77	500 HRS / 140°C / 6V No reject with std Final Test
HIGH TEMPERATURE RETENTION BAKE (1)	MIL Std 883E Method 1008	77	77	77	1000 HRS / 175°C / No Bias No reject with std Final Test

TEST	SPECIFICATIONS	LOT 1	LOT 2	LOT 3	ACCEPTANCE CRITERIA
PROGRAM EEPROM ENDURANCE CYCLING + POST RETENTION BAKE	ADCS 0061692	77	77	77	10K CYCLES @ 25°C + BAKE 72 HRS @ 175°C No reject with std Final Test
DATA EEPROM ENDURANCE CYCLING (at Hot /Ambiant/ Cold temp) + POST RETENTION BAKE	ADCS 0061692	3*77	3*77	3*77	300K CYCLES @ 85° / 25°/ -40°C + BAKE 72 HRS @ 175°C No reject with std Final Test

(1) PRECONDITIONING IS PERFORMED PRIOR TO THIS TRIAL

PACKAGE ORIENTED RELIABILITY TRIALS

TEST	SPECIFICATIONS	NUMBER OF PARTS	ACCEPTANCE CRITERIA
		1 LOT	
EXTERNAL VISUAL	JB 101	ALL	DATASHEET PACKAGE SPECIFICATIONS
PRECONDITIONING	JEDEC J-STD-20	300	JEDEC LEVEL 3
TEMPERATURE AND HUMIDITY BIAS (1)	CECC 90000	77	1000 HRS / 85°C / 85% R.H. / 5.5V
THERMAL CYCLING (1)	Mil Std 883E Method 1010	77	1000 CYCLES / -40°C TO 150°C
PRESSURE POT (1)	JA 102	77	240 HRS / 121°C / 2 ATM / 100% R.H.

(1) PRECONDITIONING WILL BE DONE ON THB, TMCL AND PPOT PARTS

Please Read Carefully: