# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN HED-AUD/07/2358
Notification Date 03/13/2007

## PDIP32 ASSY LINE TRANSFER FROM MALTA TO SUBCONTRACTOR NANTONG-FUJITSU CHINA

**AUD - AUDIO**

**Table 1. Change Identification**

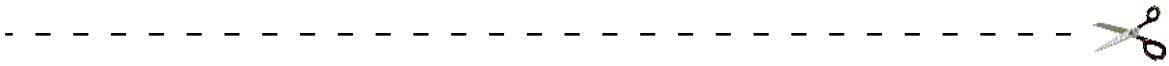
| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | TDA7442 |
| Type of change | Package assembly location change |
| Reason for change | Package rationalization |
| Description of the change | PDIP32 Malta closure and production transfer to subcontractor Nantong-Fujitsu China already qualified for this package. |
| Product Line(s) and/or Part Number(s) | See attached |
| Description of the Qualification Plan | See attached |
| Change Product Identification | "GF" as production area code for Subcon Nantong-F. |
| Manufacturing Location(s) | 1]St Kirkop - Malta |

**Table 2. Change Implementation Schedule**

| | |
|---|---|
| Forecasted implementation date for change | 01-Jun-2007 |
| Forecasted availabillity date of samples for customer | 20-Apr-2007 |
| Forecasted date for **STMicroelectronics** change Qualification Plan results availability | 06-Mar-2007 |
| Estimated date of changed product first shipment | 12-Jun-2007 |

**Table 3. List of Attachments**

| | |
|---|---|
| Customer Part numbers list | |
| Qualification Plan results | |



| Customer Acknowledgement of Receipt | **PCN HED-AUD/07/2358** |
|---|---|
| Please sign and return to STMicroelectronics Sales Office | **Notification Date 03/13/2007** |

| | |
|---|---|
| ☐ Qualification Plan Denied | Name: |
| ☐ Qualification Plan Approved | Title: |
| | Company: |
| ☐ Change Denied | Date: |
| ☐ Change Approved | Signature: |

Remark

.....

.....

.....

.....

.....

.....

.....

.....

# DOCUMENT APPROVAL

| Name | Function |
|---|---|
| Onetti, Andrea Mario | Division Marketing Manager |
| Angelici, Marco | Division Product Manager |
| Piccoli, Massimo | Division Q.A. Manager |

**PDIP32S ASSY LINE TRANSFER FROM MALTA TO SUBCONTRACTOR NANTONG-FUJITSU CHINA**

**WHAT:**
Following a Company package strategy for PDIP32S, we are on going to transfer the production of this package from Malta to subcontractor Nantong-Fujitsu China, already operative for this package.

TDA7442 is the the only Audio product involved in this transfer and we will start production in Nantong-Fujitsu as leadfree.

**WHY:**
Company package strategy for PDIP32S

**HOW:**
See attached the Reliability Report (HPC REL 12_05) that qualifies production in Nantong-Fujitsu China.
The Audio product TDA7442 must be considered qualified by extension.

**WHEN:**
From June 07 deliveries onward.

# PACKAGE RELIABILITY QUALIFICATION REPORT
# HPC REL 12_05

## HPC - MLD Groups

**REPORT NUMBER :** **HPC REL 12_05**

**QUALIFICATION TYPE :**

**DEVICE :** **TV1**
**TV2**
**TV3**

**DATE OF ISSUE :** **June 1st 2005**

| REVISION | MAIN CHANGES | DATE |
|---|---|---|
| Rev A | Initial release | June 1st 2005 |

## QUALIFICATION IDENTIFICATION:

**The object of this qualification plan is to validate the PDIPD32S lead-free package from Nantong-Fujitsu as an additional outsourcing for this package.**
**The test vehicles choice for the qualification is intending to qualify all HPC & MLD products in the PDIP32S at the time of the Change Request.**

## CONCLUSION

**All the reliability tests required for the package qualification have been successfully passed.**
**The PDIPD32S lead-free package from Nantong-Fujitsu, using pure Tin electro-plating satisfies the reliability performances necessary for the package qualification.**
**This qualification was performed according to STMicroelectronics Standard Operating Procedure 262.**

**Approved by:**

**Pascal MAURICE,**
**HPC Back-End Quality Assurance Manager**

**Francisco DE MINGO,**
**Microcontroller Quality Assurance Manager**

## PACKAGE CHARACTERISTICS

| PACKAGE FEATURES | |
|---|---|
| Package name | PDIP 32 .4 Cu .25 Shrink |
| Body sizes | 400 mils |
| Assembly site | Nantong-Fujitsu |
| Die attach | HITACHI EN4040AG |
| Molding compound | SUMITOMO EME6600CS |
| Wire material / diameter | Au / 1 mil |
| Wire bonding | Thermo-sonic |
| Frame | Copper, 155x215 & 193 x 217 |
| Electro-Plating | Pure Tin |

## TEST VEHICLES INFORMATION

| DIE FEATURES | | | |
|---|---|---|---|
| Line | TV1 | TV2 | TV3 |
| Package | PDIP32S | PDIP32S | PDIP32S |
| Diffusion process | HF3CMOS | HF3CMOS | CMOSM6XFTP |
| Wafer diameter (inch) | 6 | 6 | 6 |
| Wafer Thickness (µm) | 375 | 375 | 375 |
| Diffusion site | CARN | CARN | PHOENIX |
| Die size (mm) | 3.4 x 3.6 | 3 x 3.2 | 4.04 x 3.17 |
| Pad size (mils) | 193 x 217 | 155 x 215 | 155 x 215 |
| Ground bond | No | No | No |
| Metal | 2 | 2 | 3 |
| Passivation | P-VAPOX(SiO2) / NITRIDE | P-VAPOX(SiO2) / NITRIDE | P-VAPOX(SiO2) / NITRIDE |
| Backside finishing | LAPPED SILICON | LAPPED SILICON | LAPPED SILICON |

# 1. RELIABILITY REQUIREMENTS

The following tests have been performed in order to check the reliability performances of the package.

## RELIABILITY TESTS

| TEST | METHOD | CONDITION | Sample size/lot |
|---|---|---|---|
| **Thermal Cycling** | **MIL Std 883 Method 1010** | **-40 °C, +150 °C, 1000 Cy** | **50** |
| **High Temperature Storage** | **CECC 90000** | **85 °C, 85 % RH, 5.5 V, 1000 hrs** | **80** |
| **Pressure Pot** | **ST spec # 0061692** | **121 °C, 100 % RH, 2 Atm, 240 hrs** | **50** |
| **High Temperature Reverse Bias** | **ST spec # 0061692** | **Tamb=100°C, Tj=150°C, Vs=13.6V 1000 h** | **60** |

## RELIABILITY MATRIX & QUALIFICATION PLAN

| TEST | CONDITIONS | Readings | TV1 | TV2 | TV3 | Sample size / TV |
|---|---|---|---|---|---|---|
| ***PPT*** | ***2 atm, 121°C*** | ***168h, 240h*** | ***X*** | ***X*** | ***X*** | ***50*** |
| ***TC*** | ***-40°C/+150°C*** | ***500c, 1000c*** | ***X*** | ***X*** | ***X*** | ***50*** |
| ***HTRB*** | ***Tamb=100°C, Tj=150°C, Vs=13.6V*** | ***500h, 1000h*** | ***X*** | ***X*** | ***-*** | ***60*** |
| ***HTS*** | ***Storage 150°C*** | ***500h, 1000h*** | ***X*** | ***X*** | ***X*** | ***80*** |

# 2. RELIABILITY RESULTS

## 2.1. *PRESSURE POT*

| LOT | 168 hrs | 240 hrs |
|---|---|---|
| TV1 | 0/54 | 0/54 |
| TV2 | 0/50 | 0/50 |
| TV3 | 0/54 | 0/54 |
| TOTAL | 0/158 | 0/158 |

## 2.2. *THERMAL CYCLING*

| LOT | 500 cy | 1000 cy |
|---|---|---|
| TV1 | 0/50 | 0/50 |
| TV2 | 0/50 | 0/50 |
| TV3 | 0/50 | 0/50 |
| TOTAL | 0/150 | 0/150 |

## 2.3. *HIGH TEMPERATURE REVERSE BIAS*

| LOT | 500 hrs | 1000 hrs |
|---|---|---|
| TV1 | 0/60 | 0/60 |
| TV2 | 0/60 | 0/60 |
| TV3 | - | - |
| TOTAL | 0/120 | 0/120 |

## 2.4. *HIGH TEMPERATURE STORAGE*

| LOT | 500 hrs | 1000 hrs |
|---|---|---|
| TV1 | 0/80 | 0/80 |
| TV2 | 0/80 | 0/80 |
| TV3 | 0/80 | 0/80 |
| TOTAL | 0/240 | 0/240 |

# ANNEX 1
# Reliability tests description

| TEST NAME | DESCRIPTION | PURPOSE |
|---|---|---|
| **JLn:** Jedec Level n surface mounting simulation | The device is submitted to a typical temperature profile used for surface mounting, after controlled moisture absorption. | *As stand-alone test:* to investigate the level of moisture sensitivity.<br>*As preconditioning before other reliability tests:* to verify that the surface mounting stress does not impact on the subsequent reliability performance.<br>The typical failure modes are "pop corn" effect and delamination. |
| **TCT:** Temperature Cycles Test | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, and die attach layer degradation. |
| **PPT:** Pressure Pot Test | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |
| **HTS:** High Temperature Storage | The device is stored in unbiased condition at the max. Temperature allowed by the package materials, sometimes higher than the max. Operative temperature. | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress voiding. |
| **HdST:** Humid Storage Test | The device is stored at controlled conditions of temperature and relative humidity. | To investigate failure mechanisms activated in the die-package environment by wet conditions. Typical failure mechanisms are corrosion and surface effects related to the molding compound. |
| **H.T.R.B.: High Temperature Reverse Bias** | The device is stressed in static configuration, trying to satisfy as much as possible the following conditions:<br>-) low power dissipation<br>-) max. supply voltage compatible with diffusion process and internal circuitry limitations<br>-) max. junction temperature | This test puts in evidence potential problems related to chip stability and process contamination, verifying<br>the die-package interaction and layout weakness |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(‘‘ST’’) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE ( AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION ), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS ‘‘AUTOMOTIVE GRADE’’ MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners



STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morroco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

**www.st.com**