PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-IPC/07/2298
Notification Date 02/22/2007

2ND SOURCE ASSEMBLY & TESTING LINE OF TSM1051CLT DEVICE (1051 LINE) IN NANTONG FUJITSU SUBC (SOT23 - 6 leads)

IPC - IND.& POWER CONV.

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	TSM1051CLT
Type of change	Package assembly location change
Reason for change	capacity increase
Description of the change	see attachment
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Traceab. production area code inside marking "F"
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

Forecasted implementation date for change	15-Feb-2007
Forecasted availabillity date of samples for customer	10-Mar-2007
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Feb-2007
Estimated date of changed product first shipment	24-May-2007

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

- -

Customer Acknowledgement of Receipt	**PCN APM-IPC/07/2298**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 02/22/2007**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Menniti, Pietro	Division Marketing Manager
Gattavari, Giuseppe	Division Product Manager
Motta, Antonino	Division Q.A. Manager

2nd SOURCE ASSEMBLY & TESTING LINE OF TSM1051CLT DEVICE (1051 LINE) IN NANTONG FUJITSU SUBCON (SOT23 – 6 LEADS)

WHAT:

APM-IPC Div. is going to qualify a 2nd source b-end and testing plant in Nantong Fujitsu subcon for the device TSM1051CLT$YBE belonging to the 1051 line.

WHY:

Production rationalization and B-end capacity increase

HOW:

according to the attached qualification report

WHEN:

the production will start in Q2, 2007. The relevant samples could be available in March 2007

Q&R Project Code: ER000207CT6017

QUALITY & RELIABILITY EVALUATION REPORT

TRANSFER LINE -SOT 23-6L- TSM1051 FROM CARSEM (M) TO FUJITSU (NANTONG) PURE TIN FINISHING

Abstract

A qualification exercise it was done, to qualify the *TSM1051 on SOT23-6L Pure Tin ON FUJITSU SUBCON already qualified and in production in CARSEM (M).

Conclusion

On the basis of the already achieved positive results; Workability & testing reports, Construction Analysis Reliability evaluation, we can issued a full qualification for all the I&PC involved products on SOT 23- 6L FUJITSU (Pure Tin)

Issued by
FrancescoVentura
(I&PC QA&RB-END)

Approved by
AntoninoMotta
(I&PC /QA&R MNG)

Reliability test conditions and results for *TSM1051

N	TEST NAME	CONDITIONS [SPEC]	SAMPLE SIZE	DEFECTS*	NOTES
	Preconditioning of SMD	Preconditioning Jedec Level @1 Bake 24hrs @125°C Store 168hrs @TA=85°CRH=85% 3x reflow @260°C Electrical Testing C-SAM T-SAM	150pcs	 0 def/150 0 def/150 0 def/150	
	T.C	TC 100Cy Ta=-65°C +150°C	100	0/100	
	PPT	168hrs Ta=121°C- Pa=2Atm	100	0/100	
	E.S Preconditioning Jedec Level @1+TC	Preconditioning Jedec Level @1 Bake 24hrs @125°C Store 168hrs @TA=85°CRH=85% 3x reflow @260°C TC 100Cy Ta=-65°C +150°C	100	0/100	

* **Defect is any device rejected at the readout electrical testing or failing additional acceptance criteria according to the specified procedure.**

Device construction note

DIE FEATURES		
Die Code	:	P1051ABH
Diffusion process	:	12 HF4CMOS
Wafer diameter	:	5”
Diffusion site	:	
Die size	:	1280X800 microns
Matal level	:	1 AlSiCu .0550 micron 2 AlSiCu .0650 micron 3 AlSiCu .0850 micron
Intermetal dielectric	:	
Passivation	:	P-VAPOX(SiO2) /NITRIDE (SiN)
Back finishing	:	Raw silicon
Diffusion lot	:	X1051ABH

PACKAGE FEATURES		
Technical code	:	WB
Package name	:	SOT23-6L
Assembly site	:	FUJITSU NANTONG
Leadframe / substrate	:	SOT23-6L OPTD SELECTIVE Ag
Die attach	:	Ablebond 8200T
Wire Bonding	:	1.0 mils
Molding compound	:	MP8000-CH4
Solder balls / plating	:	N/A
Assy lot	:	
Wafer Tickness	:	280+/-25 UM

Attachments:

1) Reliability tests description (MANDATORY)

2)MBD (Mont & Bond Diagram)

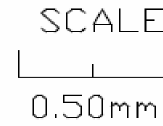
3) POA (Package Outline Assembly)

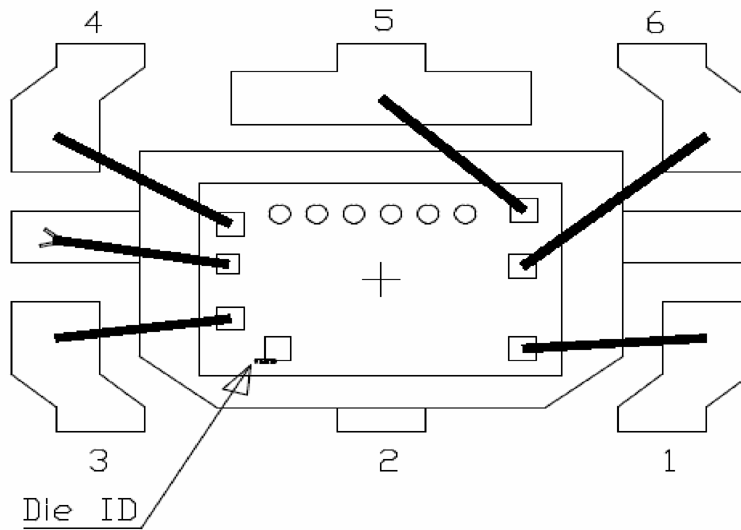
ATTACHMENT 1: RELIABILITY TEST DESCRIPTION

TEST NAME	DESCRIPTION	PURPOSE
JLn: Jedec Level n surface mounting simulation	The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.	As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TCT: Temperature Cycles Test	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.
PPT: Pressure Pot Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTS: High Temperature Storage	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
TST: Thermal Shock Test	The device is submitted to cycled thermal shocks through alternate immersion in a hot and a cold oil bath.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.
HTRB: High Temperature Reverse Bias Test	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: -) low power dissipation; -) max. supply voltage compatible with diffusion process and internal circuitry limitations; -) max. junction temperature.	To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
THB: Temperature Humidity Bias Test	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions. Typical failure mechanisms are electro-chemical corrosion and surface effects related to the moulding compound.

BONDING DIAGRAM FOR LINE : 1051 PACKAGE : WB

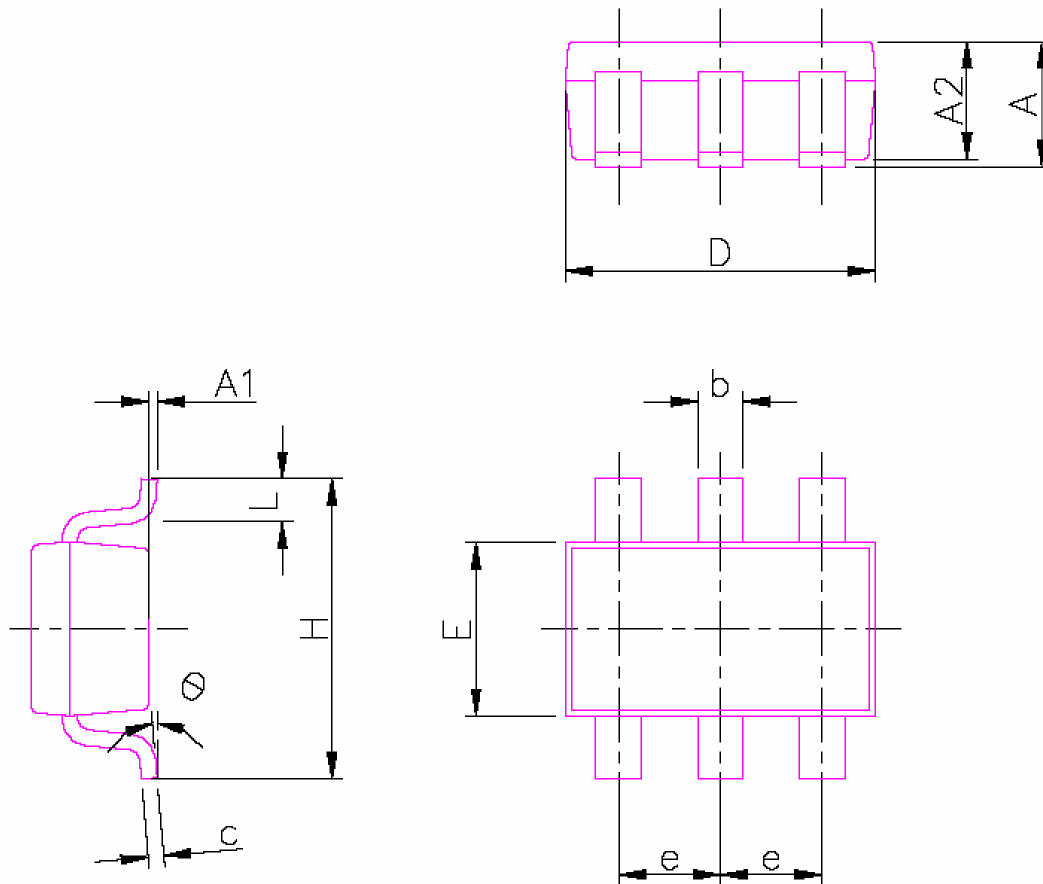
FRAME PAD : .064 x .039 inch
1.626 x 0,991 mm

SCALE


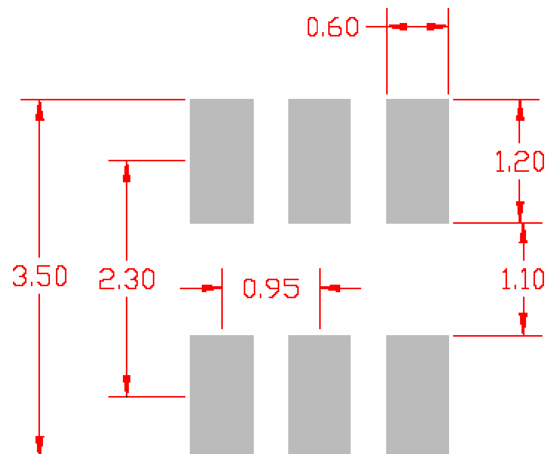


SOT23 6L (LEAD 2 FUSED)
BLANK BOND. DIAG. REF. : 5FT0043

FIGURE 1 – Package outline drawing SOT23-6L



FOOTPRINT



PACKAGE OUTLINE

PACKAGE TYPE: SOT23 6 LEADS (SUBCONTRACTOR)
PACKAGE CODE: WB
JEDEC/EIAJ REFERENCE NUMBER: MO178AB
Cotation out of JEDEC MO178AB

TABLE

				DRAWING						
REF.	**DATABOOK**			**MILLIMETERS**			**INCHES**			**NOTES**
	TYP	**MIN**	**MAX**	**TYP**	**MIN**	**MAX**	**TYP**	**MIN**	**MAX**	
A		0.9	1.45		0.9	1.45		0.035	0.057	
A1		0	0.10		0	0.10		0	0.0039	
A2		0.9	1.3		0.9	1.3		0.035	0.0512	
b		0.35	0.5		0.35	0.5		0.014	0.02	
c		0.09	0.2		0.09	0.2		0.004	0.008	
D		2.8	3.05		2.8	3		0.11	0.118	
E		1.5	1.75		1.5	1.75		0.059	0.0689	
e	0.95			0.95			0.037			
H		2.6	3		2.6	3		0.102	0.118	
L		0.1	0.6		0.1	0.6		0.004	0.024	
θ		0	10		0	10		0	10	**DEGREES**

NOTES:

1. Controlling Dimension: MILLIMETER
2. Package outline exclusive of any mold flashes dimensions and metal burrs
3. Max resin gate protusion : 0.20mm

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