PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MPA-PMT/06/2199
Notification Date 12/08/2006

Power MOSFET silicon Line optimization for the type STP75NF75

PMT - POWER MOSFET

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	STP75NF75
Type of change	Waferfab process change
Reason for change	To improve Back-End throughput
Description of the change	Die Lay-Out has been optimized to allow a new improved Bonding technique called RIBBON.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	"&" on marking area
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

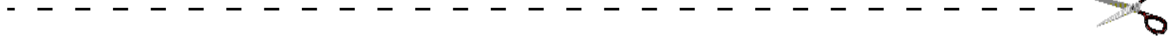
Forecasted implementation date for change	07-Mar-2007
Forecasted availabillity date of samples for customer	04-Dec-2006
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	04-Dec-2006
Estimated date of changed product first shipment	07-Mar-2007

Table 3. Change Responsibility

	Name	Signature	Date
Division Product Manager	Ian Wilson		Dec.04 ,06
Division Q.A. Manager	Giuseppe Falcone		Dec.04 ,06
Division Marketing Manager	Maurizio Giudice		Dec.04 ,06

Table 4. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt Please sign and return to STMicroelectronics Sales Office	**PCN MPA-PMT/06/2199** **Notification Date 12/08/2006**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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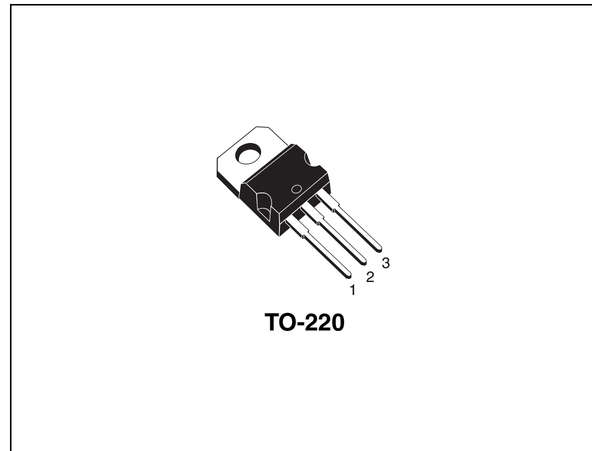
STP75NF75

N-channel 75V - 0.0095Ω - 80A - TO-220 STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STP75NF75	75V	<0.011Ω	80A

- Exceptional dv/dt capability
- 100% avalanche tested

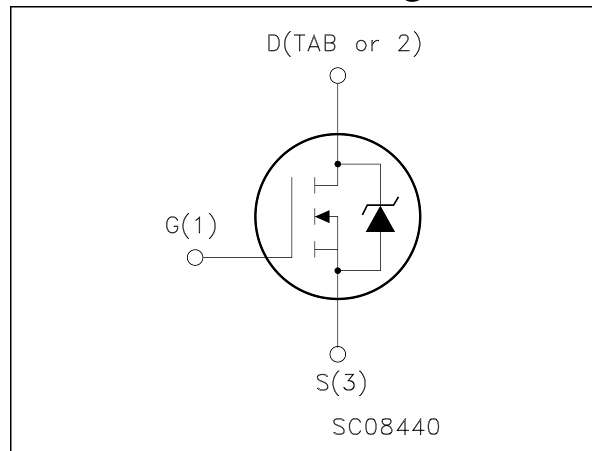


TO-220

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STP75NF75	P75NF75	TO-220	Tube

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2 Electrical characteristics 4

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	75	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	80	A
I_D	Drain current (continuous) at T_C=100°C	70	A
I_{DM} (1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25°C	300	W
	Derating factor	2.0	W/°C
dv/dt (2)	Peak diode recovery voltage slope	1.2	V/ns
E_{AS} (3)	Single pulse avalanche energy	700	J
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 80A$, di/dt $\leq 300A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
3. Starting T_J = 25 °C, I_D = 40A, V_{DD} = 37.5V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max	0.5	°C/W
R_{thJA}	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose(1)	300	°C

1. 1.6mm from case for 10sec)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	75			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 40A		0.0095	0.011	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 40A		20		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f = 1 MHz, V_{GS} = 0		3200 610 160		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 37.5V, I_D = 80A V_{GS} =10V		90 17 34		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 37.5V, I_D= 40A, R_G=4.7Ω, V_{GS}=10V *Figure 12 on page 8*		18 77 112 55		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				80	A
I_{SDM} (1)	Source-drain current (pulsed)				320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 80A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80A, di/dt = 100A/µs, V_{DD} = 20V, T_J = 150°C *Figure 14 on page 8*		91 274 6		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

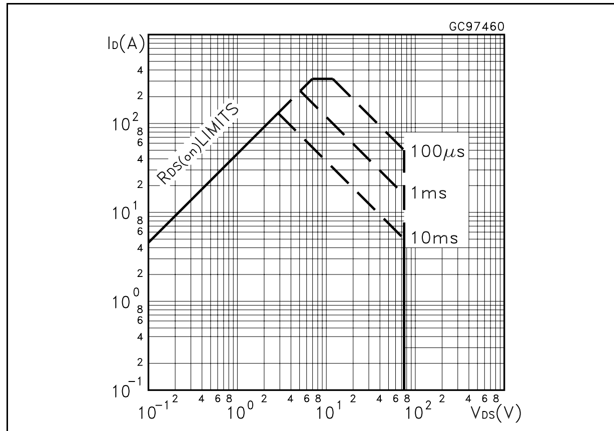


Figure 2. Thermal impedance

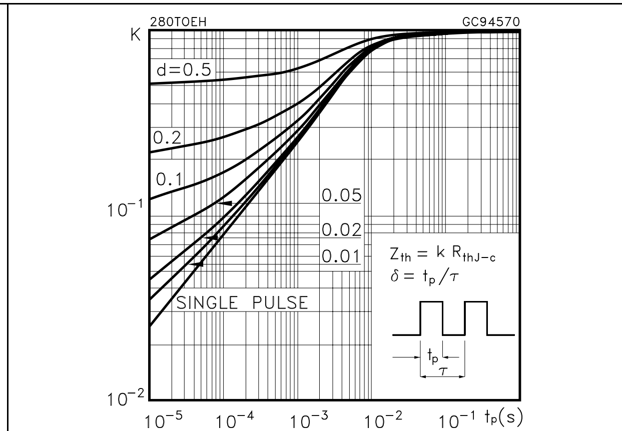


Figure 3. Output characterisics

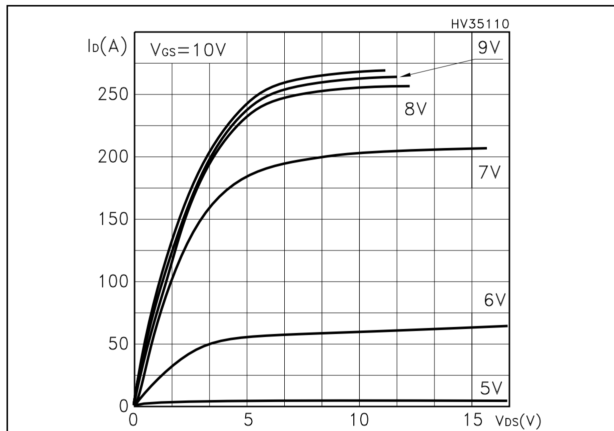


Figure 4. Transfer characteristics

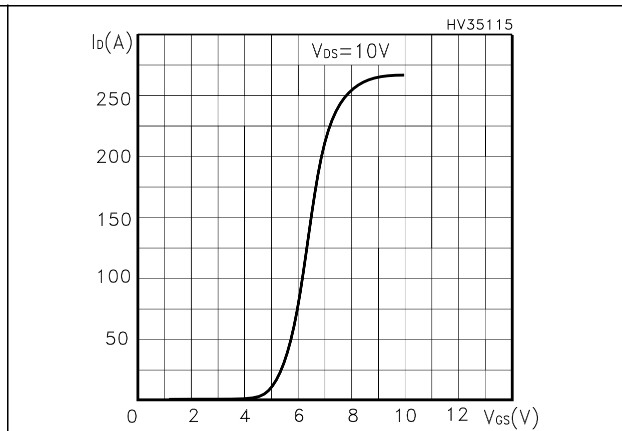


Figure 5. Normalized B_{VDSS} vs temperature

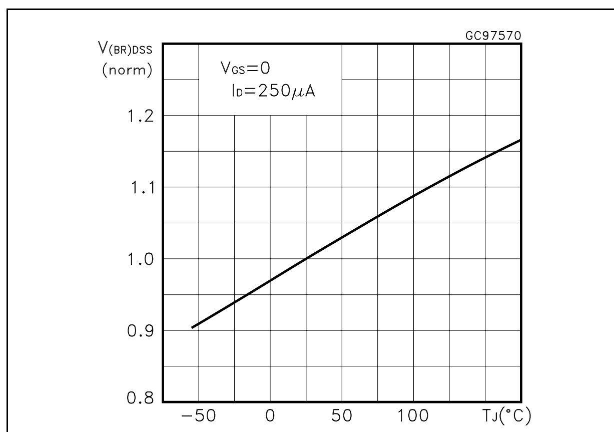


Figure 6. Static drain-source on resistance

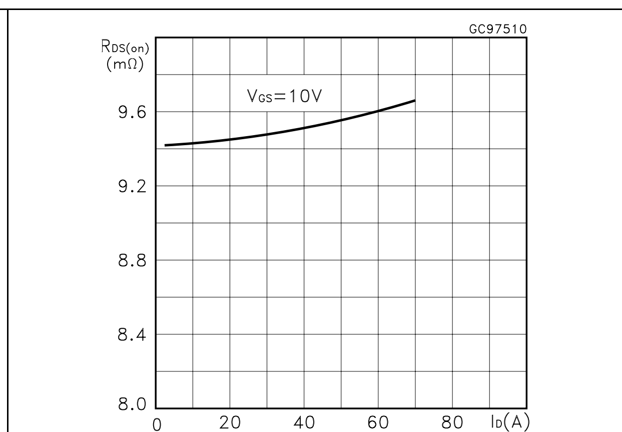


Figure 7. Gate charge vs gate-source voltage **Figure 8. Capacitance variations**

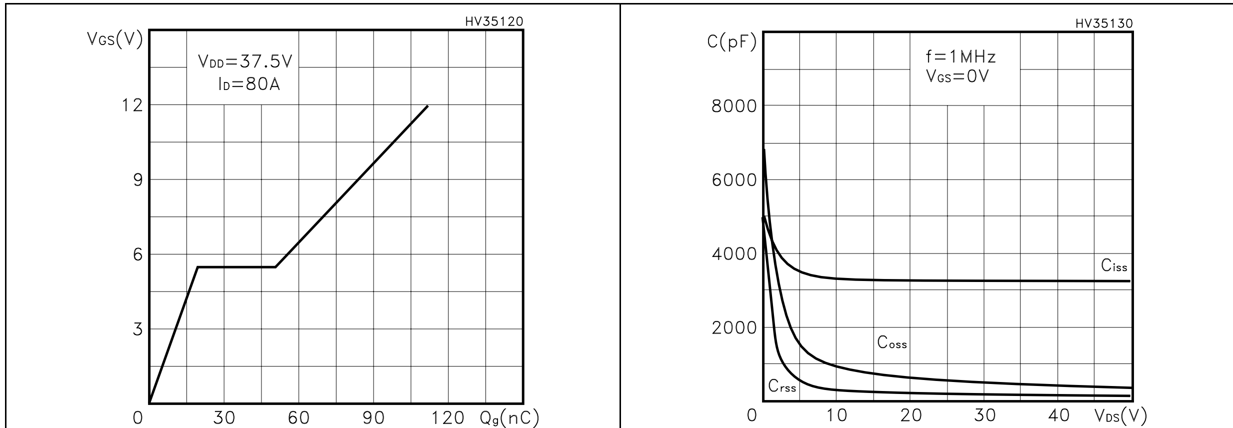


Figure 9. Normalized gate threshold voltage vs temperature **Figure 10. Normalized on resistance vs temperature**

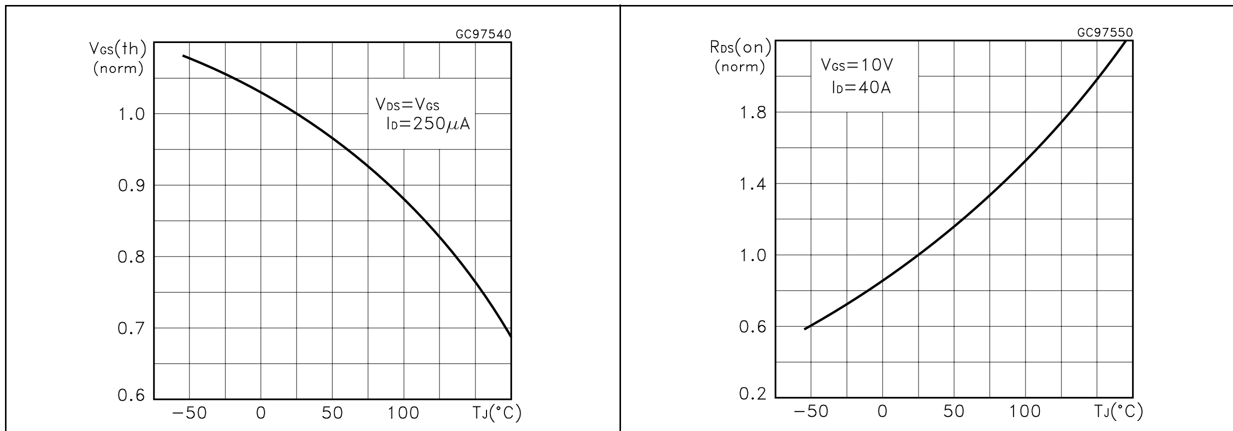
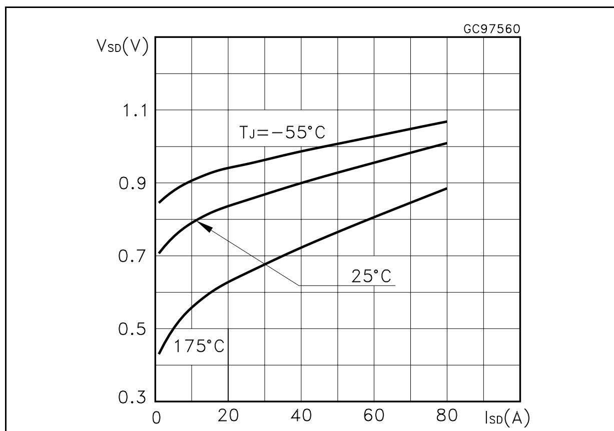


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

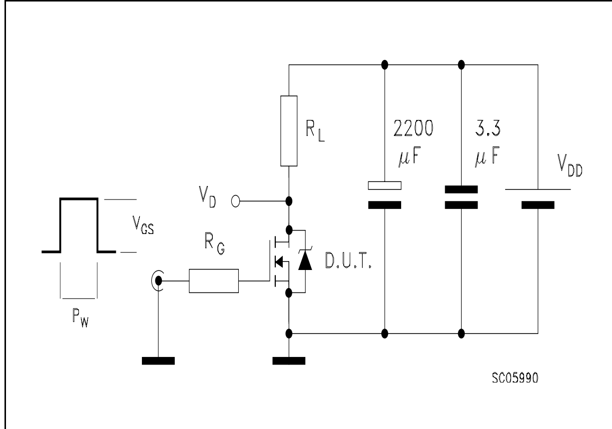


Figure 13. Gate charge test circuit

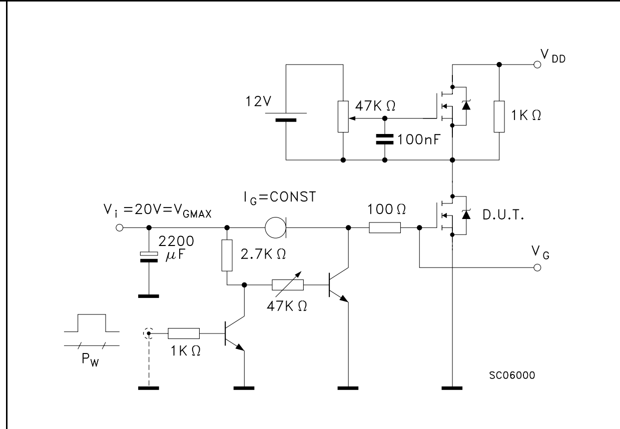


Figure 14. Test circuit for inductive load switching and diode recovery times

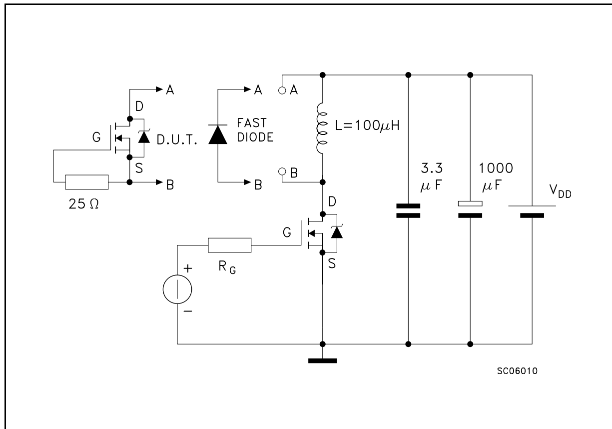


Figure 15. Unclamped inductive load test circuit

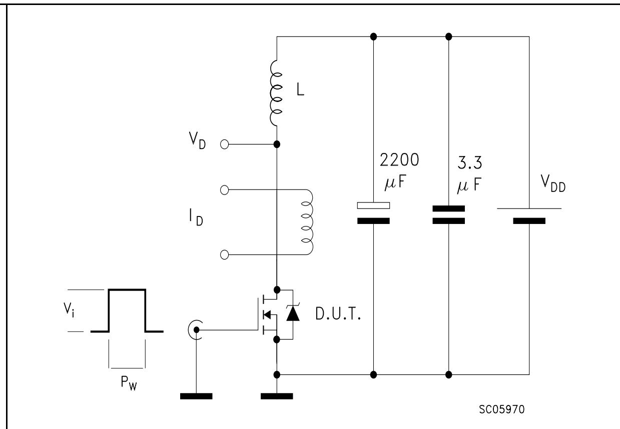
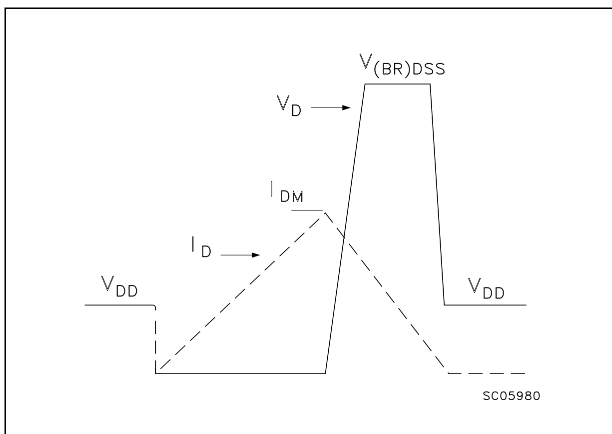


Figure 16. Unclamped inductive waveform

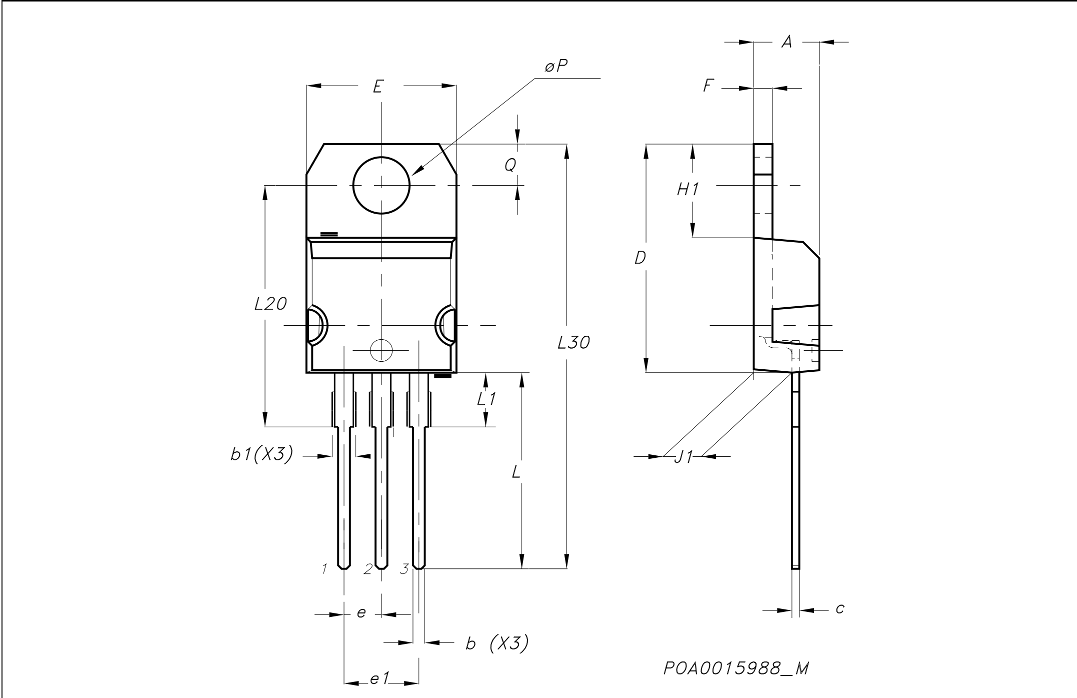


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 7. Revision history

Date	Revision	Changes
01-Dec-2006	1	First release

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RELIABILITY EVALUATION

ON

STP75NF75 with Ribbon Bonding

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Introduction

This report aims at the internal qualification of STP75NF75 N-CHANNEL STripFET™ II Power MOSFET with Ribbon Bonding.

The Qualification Reliability test trials have been performed in ST Catania Site.

The evaluation results meet ST products qualification targets, therefore the STP75NF75 N-CHANNEL STripFET™ II Power MOSFET with Ribbon Bonding is qualified.

<u>Test Vehicles</u> :

Product Line	**Sales Type**	**Package**
ED7U	STP75NF75	TO-220

<u>Failure Criteria</u> :

A failed component is a device which becomes inoperative during the test or it fails on meeting the end limits foreseen in the device specification, for one or more than the parameters here below reported

<u>Power MOSFET Main Parameters</u>

Drain Leakage Current (Idss)
Gate Leakage Current (Igss)
Threshold Voltage (Vgs(th)
Forward On Voltage (Vsd)
Drain Source On Voltage (Vds(on))
Drain Source Breakdown Voltage (Bvdss)

Reliability Evaluation Plan and results

D.U.T.: STP75NF75 Line: ED7U Package: TO-220

Test	Conditions	S.S.	Requirement	Results
H.T.S.	TA=175°C	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
T.H.B.	TA=85°C - RH=85% Vbias= 50V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
H.T.R.B.	T.A.=175°C Vdd=60V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
H.T.F.B.	TA=150°C ; Vgss=20V	77 x 1 Lot	Parameter deviation within spec. limits at 1000 hours.	No parameter deviation out of spec. limits at 1000 hours.
PRESSURE POT	TA=121°C - PA=2Atm	77 x 1 Lot	Parameter deviation within spec. limits at 96 hours.	No parameter deviation out of spec. limits at 96 hours.
THERMAL CYCLES AIR TO AIR	TA=-65°C TO 150°C 1 HOUR / CYCLE	77 x 1 Lot	Parameter deviation within spec. limits at 500 cycles.	No parameter deviation out of spec. limits at 500 cy
THERMAL FATIGUE	TC=105°C - Pd=4.75W	77 x 1 Lot	Parameter deviation within spec. limits at 10k cycles.	No parameter deviation out of spec. limits at 10Kcy.

Technological Characteristics

D.U.T. : STP75NF75 LINE: ED7U PACKAGE: TO-220

DIE	*Technology:* N-CHANNEL STripFET™ II Power MOSFET *Material:* Silicon *Metallization – Front :* Al/Si (1%) *- Back :* Ti-Ni-Au		*Passivation :* *Dimensions :*	None 4870 X 4000 um
DIE ATTACH	(with Pb/Sn/Ag)	**FRAME**	*Frame and lead material:* *Frame coating :* *Lead coating :*	Copper PINi/NiP Plating Ni/NiP Plating
WIRE BOND	Ultrasonic	**WIRE**	*Material :* *Dimension :*	Al/Mg Gate Al Source Wire 5 mils Gate Ribbon 80X10 mils Source
SEALING	Molding	**PACKAGING**	*Material :*	Epoxy Resin

PRODUCTION PLACES: WAFER PROCESSING: SINGAPORE
ASSEMBLY LOCATION: SHENZHEN
Q.A. LOCATION : SHENZHEN

Reliability Test Description

High Temperature Reverse Bias (HTRB)

This test is performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and simultaneously reverse biased. The purpose of this test is to detect surface defects such as poor passivation, presence of contaminants, etc...

High Temperature Forward Bias (HTFB)

This test is performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and simultaneously forward gate biased. The purpose of this test is to detect surface and gate oxide defects.

High Temperature Storage (HTS)

This stress test is performed to check the device life in a high temperature ambient. Specimens are put for a period of time inside a stove in free air. Detectable failure mechanisms are presence of contaminants and metal corrosion.

Thermal Cycles/Shocks

The purpose of this test is to determine the resistance of devices to exposure to extreme changes in temperature. Specimens are first placed in a suitable environment at a low temperature and then transferred to one at high temperature. Effects of thermal cycles/shocks include cracking of die, breaking of wire bonding, mechanical damage to the device case.

Reliability Test Description (continued)

Temperature Humidity Bias (THB)

This test is performed to check the device life in a high humidity ambient. Specimens are subjected to a permanent bias in a climatic chamber in the presence of steam. Detectable failure mechanisms are metal corrosion and moulding defects.

Pressure Pot

This test is performed in order to check device life in a high humidity ambient in an accelerated way. Specimens are subjected for a period of time inside an autoclave in the presence of steam and pressure. Detectable failure mechanism is metal corrosion.

Thermal Fatigue

This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress). The purpose of this test is to detect assembly defects : improper die-attach, bonding weakness and thermal mismatch among various components of the package.

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