PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MPA-MIC/06/2079
Notification Date 11/17/2006

TQFP 10X10 ADDITONAL ASSEMBLY SITE - STATS CHIPPAC (SINGAPORE)

MIC - MICROCONTROLLERS

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	See list below
Type of change	Package assembly location change
Reason for change	Need for improved production flexibility
Description of the change	Add Chippac Singapore as a qualified leadfree assembly site for TQFP 10x10 44 & 64 pins. Concerned part numbers are : ST72321x, ST72521x, ST72651x, ST7267x, ST7268x, ST72F321x, ST72F321Bx, ST72F325x, ST72F361x, ST72F561x, ST72F521x, ST72F651x, ST7L20x, STR71x, STR75x, ST72124x, ST72314x, ST72324x, ST72C124x, ST72C314x, ST72C334x, ST72F324Bx, ST72F324x, ST72F32Ax, ST72F621x, ST7FMCx. Samples availability date refers to the superset part number only. For specific samples request, please contact your local Sales or Marketing.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Country of origin : Singapore
Manufacturing Location(s)	

Table 2. Change Implementation Schedule

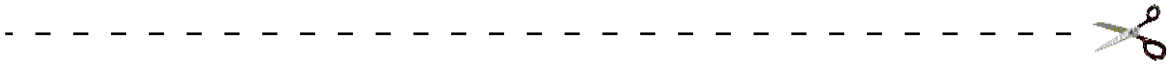
Forecasted implementation date for change	14-Feb-2007
Forecasted availabillity date of samples for customer	18-Dec-2006
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Dec-2006
Estimated date of changed product first shipment	14-Feb-2007

Table 3. Change Responsibility

	Name	Signature	Date
Division Product Manager	J. Nicholas		Nov.14 ,06
Division Q.A. Manager	F. Demingo		Nov.14 ,06
Division Marketing Manager	Y. Benmokhtar		Nov.14 ,06

Table 4. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MPA-MIC/06/2079**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 11/17/2006**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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MCD Pkg06 03 QUALIFICATION PLAN

Qualification of :

LQFP 10x10x1.4 44 Lead and 64 Lead Packages, assembled in Chippac Singapore
Pure Sn Leadfree Plating

Qualification Reference : MCD Pkg06 03

Issued on : 2/20/2006

Assembly Plant : SC STATS - SINGAPORE
Assembly Line : Standard
Package / Process : Pure Sn

Scope :

This Qualification applies to all MCD products assembled in TQFP 10x10x1.4 44 Lead and 64 Lead Packages, assembled in Chippac Singapore

Comment :

Test Vehicles :

RL Code	Number of Lots
H05W*832XXXZ	2
H04Y*811XXXY	1

Test Vehicle Features:

Die information

Test Vehicle	TV 1	TV 2
Rawline	H04Y*811XXXY	H05W*832XXXZ
psfdescr	ST72314N4 Flash	ST72561R9 Flash
Wafer Fab	ROUSSET 6'	ROUSSET 6'
FAB Process	CMOSM5S-F-DL	CMOSM6D-FTP
Die BackSide	LAPPED SILICON	LAPPED SILICON
Passivation	P-VAPOX(SiO2) / NITR	P-VAPOX(SiO2) / NITR
Die Step X	5660.00	3925.00
Die Step Y	6385.00	4560.00
Die Thickness	375	375
Pad Open X	90	90 75 90
Pad Open Y	90	90 90 75
Min Pad Pitch	150.00	135.00

Assembly information

Test Vehicle	TV 1	TV 2
raw line	H04Y*811XXXY	H05W*832XXXZ
Assembly Plant	STATS ChipPAC Ltd.	STATS ChipPAC Ltd.
Packaging	TQFP 44 10x10x1.4 1.0	TQFP 64 10x10x1.4 1
POA	0076922	0051434
BSA	CD00091976 1.0	CD00089604 3.0
B/D	7961628 A	7961622 A
Bond Placement	75% IN B.P.O.	75% IN B.P.O. 75% IN B.P.O. 75
FCA	7885645	7885645
IEDB Flow	38801	38801
Ecopack	E	E
E Mark	e3	e3
2nd Level Interco	Sn	Sn
MSL	3	3
Peak Body Temp (C)	260	260
Frame/Substrat	FRAME LQFP 10X10 44L 7.2SQ MAT Rg Ag	FRAME LQFP 10X10 64L 6.0MMSQ MAT Rg Ag
D/A Material	D/A Ablestik 3230	D/A Ablestik 3230
M/C Material	Mold - G700E	Mold - G700E
Wire	GOLD WIRE 1.0 Mils DIAM.	GOLD WIRE 1.0 Mils DIAM.

Package Reliability Trials :

Reliability Trial		Test Conditions	Pass Criteria	Unit per Lot
JL3 260	Preconditioning Level 3 JEDEC J-STD-020C	Bake (125 C / 24 hrs), Soak (30 C / 60% RH / 192 hrs), 3 x IR Reflow (260C)	3 Reflows	250
JL3+TCT	JL3+Thermal Cycling MIL Std 883, Method 1010	-40 C, +150 C	500Cy,1000Cy	50
JL3+THB	JL3+Biased Temperature and Humidity CECC 90000	85 C, 85% RH, 5.5 V	500h,1000h	80
JL3+PPT	JL3+Pressure Pot	121 C, 100% RH, 2 Atm	240h	50
SAM	SAM analysis	Delamination check : Top, Bottom Through	@ T0, J3, 240h PPT,1000Cy	15

Construction Analysis

150 extra units/lot are needed for package construction analysis

Attachment : Reliability tests description

TEST NAME	DESCRIPTION	PURPOSE
JLn: **Jedec Level n surface mounting simulation**	The device is submitted to a typical temperature profile used for surface mounting, after controlled moisture absorption.	*As stand-alone test:* to investigate the level of moisture sensitivity. *As preconditioning before other reliability tests:* to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
TCT: **Temperature Cycles Test**	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, and die attach layer degradation.
PPT: **Pressure Pot Test**	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTS: **High Temperature Storage**	The device is stored in unbiased condition at the max. Temperature allowed by the package materials, sometimes higher than the max. Operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress voiding.
THS: **Temperature Humidity Storage**	The device is stored at controlled conditions of temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by wet conditions. Typical failure mechanisms are corrosion and surface effects related to the molding compound.
TST: **Thermal Shock Test**	The device is submitted to cycle thermal shocks through alternate immersion in a hot and a cold oil bath.	To investigate failure modes related to the thermo mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moldings compound delamination, wire-bonds failure, die-attach layer degradation.

TEST NAME	DESCRIPTION	PURPOSE
THB: **Temperature Humidity Bias Test**	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions. Typical failure mechanisms are electrochemical corrosion and surface effects related to the moulding compound.
OLT: **Operating Life Test**	The device is stressed in dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature, load current, internal power dissipation.	To simulate the worst-case application stress conditions. The typical failure modes are related to electromigration, wire-bonds degradation, oxide faults.
ESD: **Electrostatic Discharge**	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models.	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU: **Latch-up**	The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effects inducing latch-up.

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