PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-CRM/06/2025
Notification Date 09/06/2006

U764 - MASK SET MIGRATION TO STEPPER EQUIPMENT

CRM - CAR RADIO & MULTIMEDIA DIV

Table 1. Change Identification

Product Identification (Product Family/Commercial Product)	SEE LIST
Type of change	Equipment change
Reason for change	Better manufacturing robustness
Description of the change	MASK SET MIGRATION TO STEPPER EQUIPMENT
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	NO MARKING CHANGE - INTERNAL TRACEABILITY
Manufacturing Location(s)	1]Amk 6"

Table 2. Change Implementation Schedule

Forecasted implementation date for change	31-Oct-2006
Forecasted availabillity date of samples for customer	04-Sep-2006
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	04-Sep-2006
Estimated date of changed product first shipment	30-Nov-2006

Table 3. Change Responsibility

	Name	Signature	Date
Division Product Manager	F. CASSANI		Sep.04 ,06
Division Q.A. Manager	L. MERCANDELLI		Sep.04 ,06
Division Marketing Manager	D. ROSSI		Sep.04 ,06

Table 4. List of Attachments

Customer Part numbers list	
Qualification Plan results	

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Customer Acknowledgement of Receipt Please sign and return to STMicroelectronics Sales Office	**PCN APG-CRM/06/2025** **Notification Date 09/06/2006**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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U764 - MASK SET MIGRATION TO STEPPER EQUIPMENT

WHAT*:*

The current U764 mask set designed on old Perking Elmer projection equipment, has been migrated to a new Stepper Canon photolithography exposition. The die circuitry & layout remain unchanged.

WHY:

Better manufacturing robustness (yield & quality).

HOW:

Attached is the report **TR0016006AG8959** qualifying the mask set for Stepper equipment .

Characterization report available on request.

WHEN:

Progressively from October 2006 onward.

Reliability Evaluation on U764 diffused in BCD2S AMK 6” with a new mask set for stepper

Abstract

The U764 device version involved in the qualification exercises, contains the two following modification:

1) new mask sets for Stepper
2) introduction of chip indexing (see attached file…..)

A set of reliability tests have been performed on one lot of U764 device in order to check that modifications in object do not introduce any weakness from reliability viewpoint .

Conclusion

The positive results obtained in the all stress test, as showed at pg. No. 2, point out that the two modifications do not introduce any weakness from reliability viewpoint on the U764 device.

Reliability test conditions and results:

N	TEST NAME	CONDITIONS [SPEC]	SAMPLE SIZE	DEFECTS*	NOTES
1	TCT	Ta=-55/+150°C Air to air 1000 cycles	50	0	1-2
2	PPT	P=2atm, Ta=121°C, t=96h	50	0	-
3	L- UP	JEDEC 78 (I injection = + 200mA) at 25°C, AEC-Q100-004- REV C	8	0	-
		The Over voltage (over VS=+24,3V) JEDEC Standard with both the conditions inputs=LOW and inputs=HIGH at 25°C, AEC-Q100-004- REV C	4	0	-

* Defect is any device rejected at the readout electrical testing or failing additional acceptance criteria according to the specified procedure.

NOTES:

1 No die Resin delamination after 1000 TC.

2 No passivation cracks observed around chip-index and tags. See Attachment No. 2 photos No. 2 and No. 3

Device construction note:

DIE FEATURES		
Die Code	:	U764CA6
Diffusion process	:	BCD60IISDM
Wafer diameter	:	6”
Diffusion site	:	AMK
Die size	:	4.45 x 5.57 mm^2
Matal level	:	2, Al/Si/Cu
Passivation	:	PSG+Silicon Nitride+PiX
Back finishing	:	CHROMIUM/NICKEL/GOLD
Diffusion lot	:	655017L

PACKAGE FEATURES		
Technical code	:	CAV2*U764CA6
Package name	:	MULTIWATT 15L
Assembly site	:	ST TOA PAYOH (Singapore)
Die attach	:	PREFORM Pb/Ag/Sn
Wire Bonding	:	2 mils
Moulding compound	:	SUMITOMO 6300
Marking	:	09362913 880B9611

Attachments:

1) Reliability test description.
2) Passivation cracks Photos
3) chip indexing

ATTACHMENT 1: RELIABILITY TEST DESCRIPTION

TEST NAME	DESCRIPTION	PURPOSE
TCT: Temperature Cycles Test	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.
PPT: Pressure Pot Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
LU: Latch-up	The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effects inducing latch-up.

ATTACHMENT 2: PASSIVATION CRACKS PHOTOS

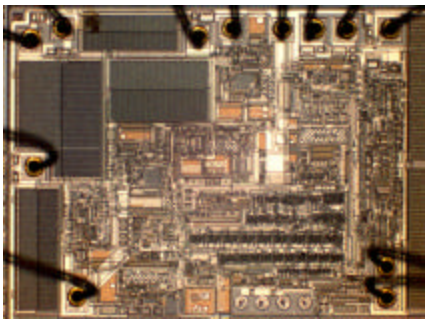

Photo No 1 (all die)

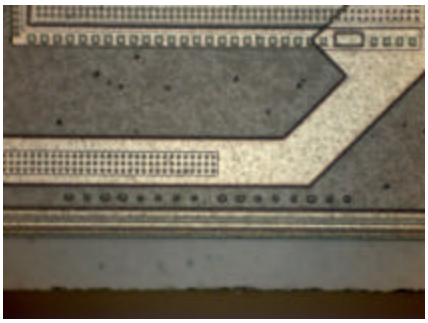

Photo No 2 (Die index)

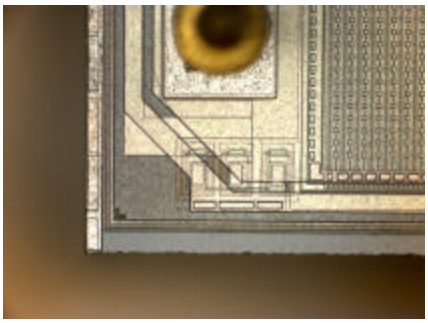

Photo No. 3 (tags)

ATTACHMENT 3: CHIP INDEXING

See next pages

CHIP INDEXING

1. Introduction

This chip indexing project was started as an APG improvement project presented during APG staff meeting in May 2005.

Chip indexing is intended to assign unique code (index) to each chip in the wafer to indicate the relative chip location within the wafer. Knowing the location of the chip within the wafer enables better analysis of failed parts. With better analysis we will be able to provide more focused corrective actions which eventually will reduce customer returns.

2. Chip Index Representation

Chip index is represented by relative row and column position of a chip within a wafer. A chip located at row *"r"* and column *"c"* on the wafer has index (*r*,*c*). Row number is increasing from top to bottom of the wafer and the column number is increasing from left to right of the wafer.

As an example, the highlighted chip in *Figure 1* is located at 7th row and 8th column therefore the index for the highlighted chip is (7,8).

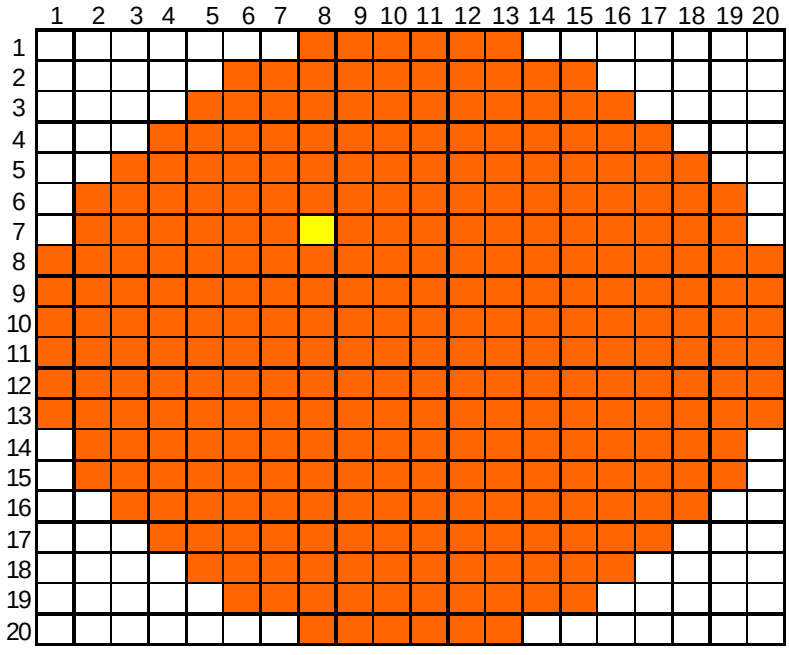

Figure 1: Index representation

3. Shape and Dimension of Chip Index Structure

Chip index has to be marked into each of chip within the wafer using as less chip area as possible to minimize intrusion into the chip area without compromising on the quality and functionality of the chip.

There is a specification intended to provide a marking symbology that can be used to mark silicon wafers i.e. SEMI T2-0298. This specification chooses a two-dimensional matrix code symbol (specified in AIM International Symbology Specification – Data Matrix) as the mark. An example of data matrix is shown in *Figure 2*.

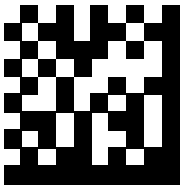

Figure 2: Data matrix example

Data matrix is not suitable to be used as chip index structure as problems like peel-off is very likely to occur due to its shape. Moreover, it has to be in considerably large size in order for it to be resolved by exposure tool.

We shall represent the index in binary code using simple and small size structure such as square (binary 0) and rectangle (binary 1).

Each chip index structure shall be composed of two sets of squares and rectangles. The first set of squares and rectangles indicates the row and the second set of squares and rectangles denote the column. The row index structures are separated from the column index structures by spacing.

For example, a chip located in the 89th row and 98th column has index (89, 98) which is (01011001, 01100010) in binary representation. The index structure for (89, 98) is illustrated in *Figure 3*.

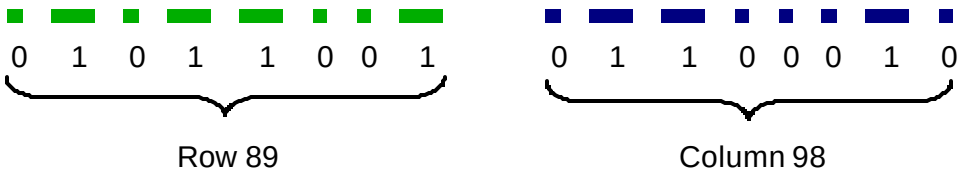

Figure 3: Index structure for (89, 98)

Up to the date when this report is written the minimum chip dimension for BCD3/BCD3S technology is 1270 µm x 740 µm (device UW30). Given a 6" (≈ 150000 µm) wafer, the maximum number of row and column we can have is 118 rows and 202 columns respectively. An eight digits binary representation can represent up to 255 rows and columns.

As already explained, the square structure denote digit 0 and the rectangle structure denote digit 1. Square structure has width and height of 4 µm while rectangle structure has width of 6 µm and height of 4 µm. The spacing from center to center of two index structures is 12 µm as shown in *Figure 4a*, *Figure 4b* and *Figure 4c.*

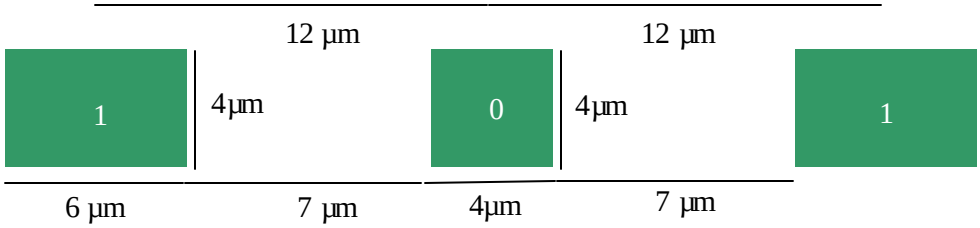

Figure 4a: Chip index spacing

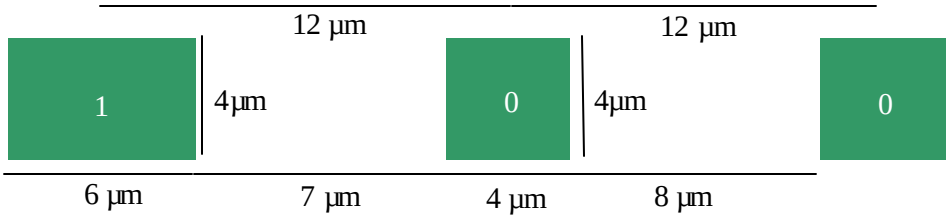

Figure 4b: Chip index spacing

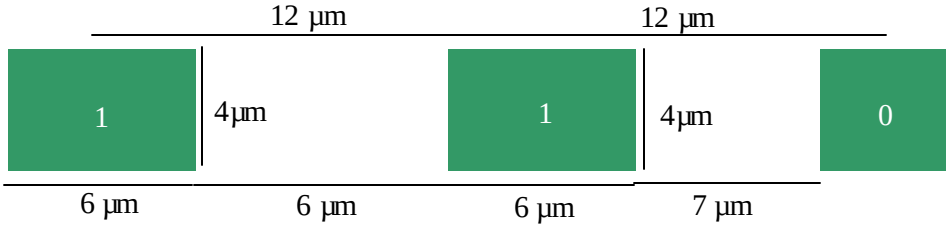

Figure 4c: Chip index spacing

The row index structures are separated from the column index structures by a 19 um spacing measured from the centre of the last digit structure in the row index to the centre of the first digit structure in the column index as depicted in *Figure 5*. The total length of the index structure can be 191 um, 192 um or 193 um. The maximum length of the index structure is 193 um and the maximum height of the index structure is 4 um.

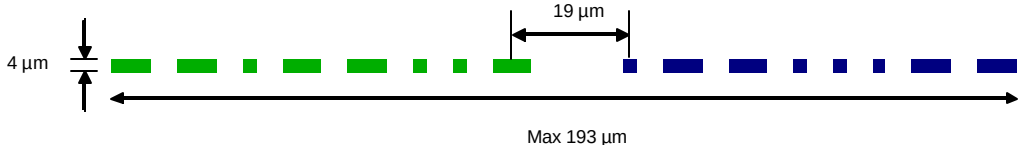

Figure 5: Index structure dimension

4. Placement of Chip Index Structure

Chip index structure shall be located within 25 µm from the edge of the chip beside the guard ring, and not touching the scribing line. After much analysis, the best positioning of chip index structures is between the device edge structures and the edge of the die, where there is a free region of approximately 20 µm. This will thus ensure that chip index structure is not inserted too close to Metal 3 internal strip as shown in *Figure 6*, taking an example of device CU764C.

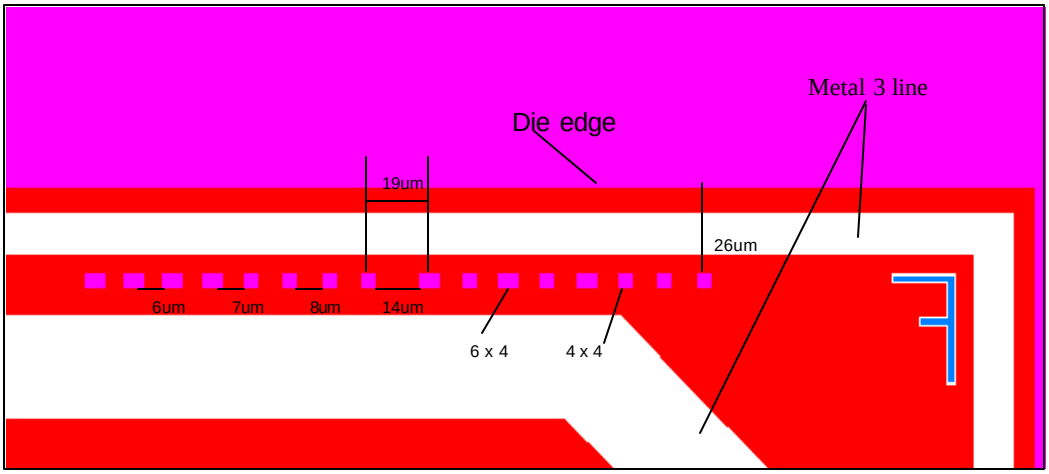

Figure 6: Location of chip index structure after overlapping with metal 3

With chip index structures placed in the above location, no modifications are needed at litho process.

Chip index structure shall be applied on only one of the mask that uses full projection lithography (e.g. Perkin Elmer) among a product maskset.

For technologies with full set projection lithography (Bipolar, BCD1 and BCD2), chip index can be applied on any one of the mask level except contact, metal, via, pre epi and PIX mask.

For technologies with mix and match exposure tools (BCD2S and BCD3) chip index can be applied on passivation mask.

The polarity of chip index is always dark. For AMK, chip index is always implemented only on passivation mask level 900.

Chip index implementation on mask 900 will cover all the three options of BCDXX passivation:

- Inorganic mask 900
- Inorganic + organic (PIX) mask 900 double etch PIX + Passivation
- Inorganic + organic (PIX) mask 900 + 950

5. Implementation and Findings of Chip index Structure

The above chip index structure has been implemented in test vehicle CU764C-900A3 and short loop trial has proven that the appearance of the chip index is good on wafer after process.

This version of chip index is further implemented on next product vehicle CUE32B-900A2.

Time line for C.I. implementation on key APG products will be defined after the above test vehicles have been qualified.