UnitedSiC | Technical Blog

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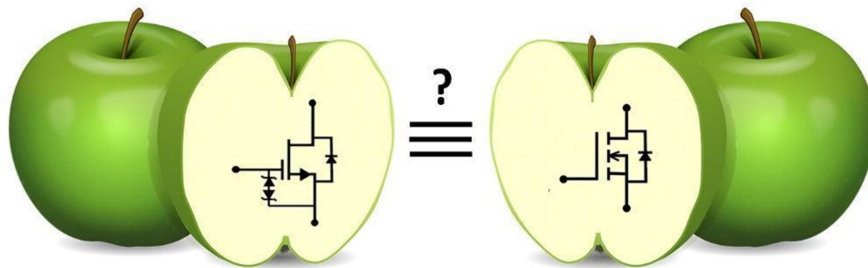
SiC FET on-resistance variation with temperature – making the right comparison

Abstract

Comparing data sheets for SiC switches can be difficult. SiC MOSFETs can appear to be at an advantage with a lower temperature coefficient of on-resistance, but this is an indicator of higher underlying losses and overall lack of efficiency compared with UnitedSiC FETs.



'Comparisons are odious' as the proverb goes, first recorded around 1440 in John Lydgate's 'Debate between the horse, goose, and sheep'. Livestock apart, designers of modern power converters have to try to dispassionately compare power switches for their application from a slew of competing claims for 'best performance'. The problem is comparing apple with apples, continuing the farming metaphor, as no single electrical parameter can be said to be better without considering its trade-off with other measures. Switch on-resistance is a good example - you have to compare parts with the same voltage rating, at the manufacturers' recommended gate drive voltage, at the same junction temperature and drain current and in the same package.

Si-MOSFETs, SiC-MOSFETs and SiC FETS vie for position

At higher voltages, from a few hundred of volts upwards, Si MOSFETs, SiC MOSFETs and UnitedSiC FETs are vying for position, with datasheets typically giving an $R_{DS(ON)}$ value at a particular voltage rating, junction temperature and gate drive voltage. Part UJ4C075018K4S recently released by UnitedSiC for example, gives on-resistance values at V_{GS} = 12V and at

25°C to 175°C, all at 20A drain current. From this you can easily derive a figure for temperature coefficient of $R_{DS(ON)}$ at a given temperature for this part that turns out to be around +70-75% at Tj =125C.

A champion of 650V SiC MOSFETs might point out that they see a figure of typically +20-25% at Tj =125C for an otherwise similar device. Is that three times better? Firstly, some positive value of temperature coefficient is necessary to force cells in a die to share current without hot-spots and thermal runaway. Similarly, designers rely on the positive value to be able to parallel devices with natural current sharing.

SiC MOSFET resistance is dominated by its inversion channel

The lower value for $R_{DS(ON)}$ temperature coefficient of SiC MOSFETs is actually an indication of a deeper effect that is happening; MOSFETs and JFETS are 'single-carrier' devices with electron flow through different regions – substrate, drift layer, JFET regions and channel etc. In a 650V SiC MOSFET, the inversion channel dominates the total resistance which actually reduces with temperature. Channel resistance is inversely proportional to (number of free carriers x electron inversion layer mobility) and as temperature rises, threshold voltage decreases and the number of free carriers in the channel increases, therefore resistance decreases. This effect is offset by the positive temperature coefficient of the rest of the device regions, namely the JFET, drift layer and substrate resistance, to produce a slight net positive Tc value. In a SiC JFET, there is no inversion channel to offset the positive temperature coefficient of the JFET, drift layer and substrate. Meanwhile, the low voltage Si MOSFET represents only a small portion of the total on-resistance, explaining the higher Tc value than with a SiC MOSFET, but the telling point is that the losses associated with the non-ideal SiC inversion layer are also absent in the SiC FET (**Figure 1**).

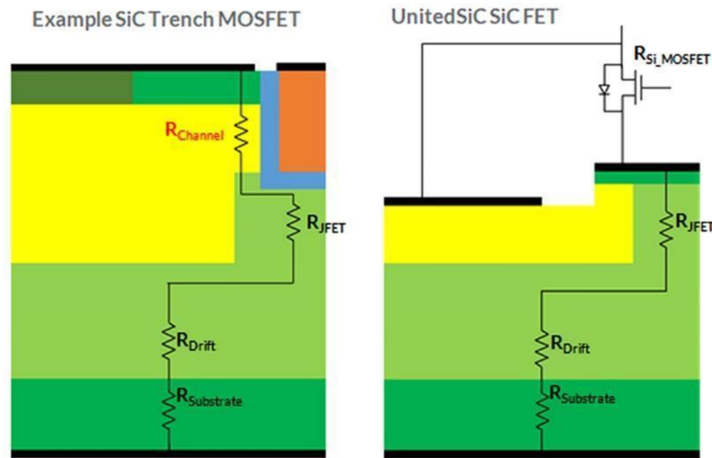


Figure 1: Typical SiC MOSFET trench construction and a UnitedSiC FET showing absence of lossy SiC MOS inversion channel leading to higher temperature coefficient of on-resistance but lower losses

SiC FETs have lower overall conduction losses

The clincher comes when you look at absolute values. As you can see in Figure 2, comparing $R_{DS(ON)}$ for 650/750V devices, the UnitedSiC FET starts at 25°C with around a third of the specific on-resistance of the SiC MOSFET and is still nearly 2x better at 150°C, with about half the consequent conduction losses for the same active die area.

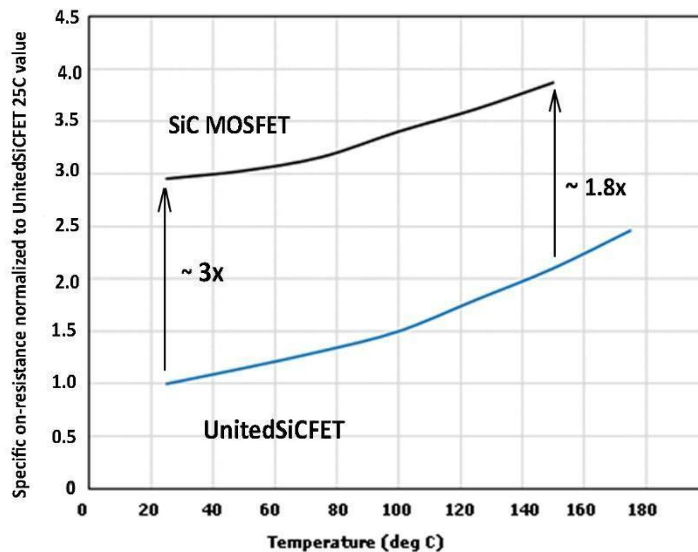


Figure 2: UnitedSiC FETs have higher Tc of on-resistance but lower absolute values

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The net effect is that there are lower overall conduction losses with a UnitedSiC FET and a healthy positive temperature coefficient of $R_{DS(ON)}$ to ensure effective current sharing between cells and paralleled devices. It clearly pays to make sure comparisons are valid and to understand the mechanisms behind the effects – it can reveal what matters practically: lower overall loss.

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